NEW

2016

BCA

2nd Semester Examination

COMPUTER ORGANZATION & ARCHITECTURE

PAPER—1201

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer Q. No. *1* and any *four* from the rest.

1. Answer any *five* questions : 5×2

(a) What do you mean by universal shift register ?

(b) State De Morgan's law.

(c) What is DMA ?

(d) What is Flash Memory ?

(e) Define Virtual Memory.

(f) Write down the disadvantages of one address instruction.

(g) The program counter (PC) is called "Memory Pointer"– Justify your answer.

2. (a) Explain floating point representation of numbers with examples.

(b) Explain the basic ideas of program execution.

(c) What are the differences between SRAM and DRAM ? Why a DRAM Cell needs refreshing ?

(d) What do you mean by Miss Penalty ? 3+3+(4+3)+2

3. (a) What is programmed I/O technique ? Why it is not very useful ?

(b) Explain the different modes of data transfer between the processor and the peripherals.

(c) Define special purpose registers and general purpose registers with examples. (2+3)+6+4

4. (a) What is addressing mode ?

   (b) Explain Base register addressing mode, Relative addressing mode and direct addressing mode.

   (c) Explain Booth's algorithm with the help of a flowchart.

2+6+7

5. (a) What is instruction format ?

   (b) Explain the general register organisation with a common ALU.

   (c) How does control word works ?

2+8+5

6. (a) Explain in detail the different types at addressing modes.

   (b) Compare RISC with CISC architecture.

   (c) Explain the difference between hardwared and microprogrammed control unit.

7+4+4

7. Write short notes (any *three*) : 3×5

(a) DMA controller ;

(b) Set-associative mapping ;

(c) Shift register ;

(d) Zero address instruction ;

(e) Interrupts.

[Internal Assessment — 30]