**NEW**

**2016**

**BCA**

**1st Semester Examination**

**DIGITAL ELECTRONICS LAB**

**PAPER—1197 (Set-3)**

**(PRACTICAL)**

*Full Marks :* 100

*Time :* 3 Hours

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

*Illustrate the answers wherever necessary.*

Answer any *two* questions (*Lottery Basis*). 2×30

**1.** Implement a half adder circuit using NOR gates only. 30

2. Design a 16 bit adder using two 7483 ICs. 30

3. Design and implement 4 bit BCD adder using 4 bit binary address. 30

4. Implement Excess-3 subtractor circuit using binary subtractor. 30

5. Design and implement a binary multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders. 30

6. Implement the function $F(ABCD) = \sum m(0,2,6,8,9,11,13,15)$ using 8 : 1 MUX. 30

7. Design a 4 bit being synchronous counter with D flip-flops. 30

8. Design a MOD-10 counter with states 0, 1, 2, 3, 4, 8, 9, 10, 11, 12. 30

9. Design a MOD-16 synchronous count up counter using J-K F/F. 30

**10.** Implement the following using ROM

$$F_1(A,\bar{B},C) = \sum m(0,2,4,7)$$

$$F_2(A,B,C) = \sum m(1,3,5,7)$$ 30

**11.** Design a Counter with the following repeated binary sequence 0, 1, 2, 3, 4, 5, 6 using J-K F/F. 30

**12.** Draw the logic diagram of a 4 bit register with four DEF and four 4×1 MUX with mode selection input $S_1$ and $S_0$, The register operates according to the following function table.

$S_1$ $S_0$

0 0 – No charge

0 1 – Implement of four output.

10 – clear register to 0.

11 – load parallel data.

## INSTRUCTIONS

### Distribution of Marks :

| | | |
|---|---|---|
| *Theory* | : | *10* |
| *Circuit* | : | *05* |
| *Implementation* | : | *10* |
| *Verification* | : | *05* |
| | *Total :* | *30* |

*Viva* — *05*

*PNB* — *05*

*[Internal Assessment — 30]*