NEW

2015

BCA

1st Semester Examination

DIGITAL ELECTRONICS LAB

PAPER—1197 (Set-2)

(PRACTICAL)

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *two* questions taking *one* from each group (*Lottery Basis*). 2×30

Group—A 1×30

1. Design NOT, OR, AND, XOR, XNOR gates using minimum number of NOR gates. 30

2. Design a half adder using NOR gates and also design Full Adder using two half-adders. 15+15

3. Design 8 to 3 encoder circuit and verify its result using only 2 input basic gates. 15+15

4. Design a full subtractor circuit & implement it using NAND gates only verify the truth table [*using minimum no.of gates*]. 25+5

5. Design a circuit to convert BCD to Excess-3. 30

6. Design a 4 : 1 MUX using minimum number of NAND gates. Verify its truth table. 30

7. Design gray code to BCD converter and verify the truth table. 30

8. Simplify the following function using K-map :

$$G = \sum m(0, 5, 7, 13, 14, 15).$$ 30

9. Design a four bit 2's complement subtractor using 1C 7483 & XOR gates. 30

10. Design 2 bit comparator circuit using suitable gates and verify the truth table. 25+5

Group—B

1×30

1. Design a 4 bit bidirectional shift register. 30

2. Design asynchronous up counter of the following MOD by using IC 7476 :

   (i) MOD 7 ; (ii) MOD 10 ; (iii) MOD 12. 30

3. Design AND and OR operation using DTL and establish its truth table. 30

4. Design a 4 bit bidirectional shift register. 30

5. Design asynchronous up counter of the following MOD using IC-7476 : 30

   (i) MOD 10

   (ii) MOD 5

6. Design a clocked SR and J-K flip-flop with present and clear using NAND gates only. 30

7. Design a J-K Master Slave flip-flop and verify its result. 30

8. Design a ripple counter using J-K flip-flop. 30

9. **Design** a synchronous counter which cycles through

$$7 \rightarrow 3 \rightarrow 4 \rightarrow 0 \rightarrow 5 \rightarrow 7$$

using J–K flip-flop and verify it. 30

10. **Design** a Buffer register and show the following result :

Input = 1010

Output = 1010 30

INSTRUCTIONS

Distribution of Marks :

Theory	:	10
Circuit	:	05
Implementation	:	10
Verification	:	05
Total	:	30

Viva — 05

PNB — 05

[Internal Assessment — 30]