NEW

2015

BCA

1st Semester Examination

DIGITAL ELECTRONICS LAB

PAPER—1197 (Set-1)

(PRACTICAL)

Full Marks : 70

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *two* questions taking *one* from each group (*Lottery Basis*). 2×30

Group—A 1×30

1. Simplity the following function using k-map.

$\sum(3, 4, 5, 7, 9, 13, 14, 15)$ 30

2. Implement $y = \overline{AB} + A + \overline{(B + C)}$ using NAND gates and verify its truth table. 30

3. Implement NOR, AND, OR, X-NOR, gates using NAND gates only and verify the truth tables. 20+10

4. Design a 4:1 MUX using minimum number of NAND gates and verify its truth table. 30

5. Design Gray Code to BCD converter and verify the truth table. 25+5

6. Design 8 to 3 encoder circuit and verify its result. (Use 2 input basic gates). 30

7. Design 2 bit comparators circuit using suitable circuit and implement it. Verify its truth table. 25+5

8. Draw and implement the logic circuit to verify the following boolean function using basic gates :

   (i) $XY + XZ + Y\bar{Z} = XZ + Y\bar{Z}$

   (ii) $(X + Z)(\bar{X} + Y) = XY + \bar{X}Z$

15+15

9. Desigm a half adder using NAND gates and design a *Full* adder using two half adders. 15+15

10. Design an excess 3 to BCD converter circuit and verify its truth table. 30

Group—B 30×1

1. Construct clocked S–R F/F uising NAND gates and verify its operation. 30

2. Design a 4 bit bidirectional shift register. 30

3. Design 4 bit ripple counter using J-K flip flop. 30

4. Design and implement right shift register and verify the operation. 25+5

5. Construct astable multivibrator using IC 555 timer. Measure its frequency and duty cycle by CRO. 30

6. Design asynchronous up counter of MOD 7 counter. 30

7. Design J–K master-slave F/F & verity its excutation table. 30

8. Design 4 bit SISO register using D flip-flop and verify the output. 30

9. Design asynchronous up counter of the following MOD using IC 7476 :

   (i) MOD 11 ; (ii) MOD 10 ; (iii) MOD 5. 30

10. Design ANO and OR operation using DTL and establish its truth table. 30

INSTRUCTIONS

Distribution of Marks :

Theory	:	10
Circuit	:	05
Implementation	:	10
Verification	:	05
Total	:	30

Viva — 05

PNB — 05

[Internal Assessment — 30]