NEW

2015

BCA

1st Semester Examination

DIGITAL ELECTRONICS

PAPER—1104

Full Marks : 70

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer *Q. No. 1* and any *four* from the rest.

1. Answer any *five* questions : 5×2

(a) What do you mean by Weighted Code ? Give example.

(b) Convert : $(10111)_2 = (?)_{Gray}$.

(c) Perform the following Addition of decimal numbers using BCD addition : 8 & 9.

(d) Define Synchronous counter.

(e) What is meant by Propagation delay in F/F ?

(f) In what condition the XOR gate acts as a Buffer.

(g) What is clock pulse ?

2. (a) What is full subtractor ? Design and draw the circuit of full subtractor using only NAND gate. 5

(b) Realize a look-ahead-carry adder. 3

(c) Design a 3-bit binary to gray converter. 5

(d) What is parallel adder (draw only block diagram with full adders) ? 2

3. (a) Distinguish between an encoder and a decoder. 3

(b) Draw a logic diagram for an Excess-3- to decimal decoder. Inputs and outputs should be active high. 5

(c) Why De-Mux is called Data distributor ? 2

(d) Implement the following logic function using Mux : $F(A, B, C, D) = \Sigma m(1, 3, 4, 11, 12, 13, 14, 15)$. 5

4. (a) How can a Decoder are used as a Demultiplexer ? 2

(b) Implement following expression using active low decoder : 3

$$Y = A\bar{B} + B\bar{C} + ABC$$

(c) Design and explain octal to binary encoder. 5

(d) Describe successive approximation method for A/D converter. 5

5. (a) Design and explain a J-K flip-flop mode by only NAND gates. 5

(b) Convert a DFF into TFF. 4

(c) What is race around condition ? How this condition will be removed ? 2+1

(d) Draw MS JK FF. 3

6. (a) Design a 3-bit even synchronous counter. 5

(b) Design a MOD-6 counter using a synchronous counter. 5

(c) Draw and explain Serial in – Serial out (SISO) shift register. 5

7. (a) What are the difference between A/D & D/A converter ? 2

(b) Draw a AND gate using DTL.

(c) What are the difference between DTL, TTL & ECL ? 3

(d) What do you mean by EPROM ? 2

(e) Implement $Y = A\bar{B} + ABC$ using NOR gate. 3

———