NEW

2015

BCA

2nd Semester Examination

COMPUTER ORGANZATION & ARCHITECTURE

PAPER—1201

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer Q. No. *1* and any *four* from the rest.

1. Answer any *five* questions : 5×2

(a) Why NOR gate is called universal gate ?

(b) State the instructions used in STACK.

(c) What disadvantage does RISC architecture possess ?

(d) What is an impedance state ?

(e) Prove De Morgan's law using boolean logic.

(f) What do you mean by micro-instruction ?

(g) Explain the use of Karnaugh Maps.

2. (a) Explain the difference between micro-programmed and bandwired control.

(b) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

(i) How many selection inputs are these in each multiplexer ?

(ii) What size of multiplexer needed ?

(iii) How many multiplexers are there in the bus ?

Deferred your answer with an appropriate logic.

6+9

3. (a) How associative memory differs from any other memory ?

(b) Briefly explain the hardware organization and working procedure of associative memory with the help of a block diagram.

5+(5+5)

4. (a) Write a programme to evaluate the arithmetic statement :

$$X = \frac{A-B+C*(D*E-F)}{G+H*K}$$

(i) Using a general register computer with three address instruction ?

(ii) Using a general register computer with two address instruction.

(b) Briefly explain the stack organization in computer memory. Also, state how the different operations are preferred on this stack.

6+9

5. (a) Draw the block diagram of 4-bit arithmetic circuit.

(b) Deduce the different arithmetic function performed by the above circuit.

(c) Can a decoder be a replacement for multiplexer ? State your reason.

(d) How selective-complement operations differs from selective-clear operations ?

3+5+4+3

6. (a) Briefly explain the general register organization with a common ALU.

(b) How does control word works ?

(c) Why DMA is necessary ? 7+4+4

7. Write short notes (any *three*) : 3×5

(a) Hardware implementation for signed-magnitude addition and subtraction ;

(b) Cache Memory ;

(c) RISC & CISC ;

(d) Flip–Flops ;

(e) Addressing Mode.

[Internal Assessment — 30]

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