NEW

2015

BCA

1st Semester Examination

DIGITAL ELECTRONICS LAB

PAPER—1197 (Set-3)

(PRACTICAL)

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *two* questions taking *one* from each group (*Lottery Basis*). 2×30

Group—A 1×30

1. Design a half adder circuit and implement it with NAND gates only. Verify the truth table.

2. Design a 3 to 8 line decoder using any gates of your choice & verify the truth table.

3. Design a 2 input XOR gate NOR gates and verify the truth table.

4. Design a 4×1 MUX using minimum no. of NAND gates only. Verify the truth table.

5. Design an Excess 3 code to BCD converter circuit and implement it. Verify the truth table.

6. Design a four bit 2's complement subtractor using IC 7483 and XOR gates.

7. Show the output logic stats of the following function :

$$f.(A, B, C) = AB + \bar{A}C + BC .$$

Group—B 1×30

8. Design a JK master slave flip-flop & verify it's operation.

9. Design a 4 bit binary ripple counter. Verify it's operation.

10. Design 4 Serial in Serial Out (SISO) register using D flip-flop and verify the output.

11. Design & implement a 4-bit bidirectional shift register.

12. Design a synchronous counter which cycles through the $7 \rightarrow 4 \rightarrow 5 \rightarrow 0 \rightarrow 6 \rightarrow 7$ using JK flip-flop. Verify your implementation.

13. Design a D-flip-flop using T flip-flop verify it's truth table.

14. Construct Astable Multivibrator using 1C-555 timer. Measure it's frequency & duty cycle by CRO.

INSTRUCTIONS

Distribution of Marks :

Theory	:	10
Circuit	:	05
Implementation	:	10
Verification	:	05
Total	:	30

Viva	**—**	***05***
PNB	**—**	***05***

[Internal Assessment — 30]