OLD

2015

Part I 3-Tier

ELECTRONICS

PAPER—I

(General)

Full Marks : 100

Time : 3 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Group—A

Answer any *two* questions. 2×15

1. (a) 'The energy levels of an atom produce energy bands in a solid'. Explain. 4

(b) What are the factors determining : (i) the width of an energy band in a crystal and (ii) the number of energy levels in the band ? $2\frac{1}{2}\times 2$

(c) Draw the energy-band diagram and position of Fermi level for : (i) p-type material, (ii) n-type material and (iii) unbiased p-n junction. 2×3

2. (a) How is a transistor represented as a two-port device ? 3

(b) Define the hybrid parameters for a basic transistor circuit in any configuration and give its hybrid model. 4+2

(c) What is Darlington connection ? Compare between an emitter follower and a Darlington pair. 3+3

3. (a) Explain the concept of feedback in amplifiers. Find out an expression for the voltage gain with feedback. 3+3

(b) Explain under what conditions a positive feedback amplifier gives oscillations. 3

(c) Draw the circuit diagram of a Wien-bridge oscillator with an operational amplifier as an active element. Mention the advantages and disadvantages of the Wien-bridge oscillator. 3+3

Group—B

Answer any *five* questions. 5×8

4. (a) How are the width of space-charge region and the barrier height affected when a p-n junction is : (i) forward-biased, (ii) reverse-biased ?

$2\frac{1}{2}\times 2$

(b) Calculate the ratio of the current for a forward bias of 0.06V to the current for the same value of reverse bias applied to a Ge p-n diode at 27°C. 3

5. (a) Draw the circuit diagram for studying the static characteristics of a p-n-p transistor operation in CE mode. 2

(b) Sketch two important characteristics for the CE mode and explain them. 3×2

6. (a) Compare between a FET and a BJT. 4

(b) An n-channel JEFT has I_{DSS} = 12mA and pinch-off voltage V_P = −4V. Find the drain current for V_{GS} = −2V. If the transconductance G_{mo} of a JFET with the same I_{DSS} at V_{GS} = 0 is 4 millimho, find the pinch-off voltage. 2+2

7. (a) Draw a circuit diagram of a push-pull power amplifier. 3

(b) Obtain an expression for the maximum efficiency of the circuit. 5

8. (a) Draw the structure and device symbol of a triac. 2+1

(b) Discuss the principle of operation of triacs and name their uses. 4+2

9. (a) Find the Thevenin and Norton equivalent circuit between the terminals a, b for the network of Fig. 1 : 3+3

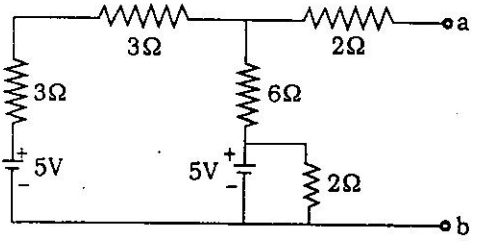

Fig. 1

(b) Determine the resistance to be connected across a, b in Fig. 1 to dissipate maximum power and calculate the maximum power. 1+1

10. (a) A battery of voltage V_0 is switched on to a series combination of a resistor R and an initially uncharged capacitor c at time t = 0. Calculate (i) the energy stored in the capacitor when it is fully charged ; (ii) the energy dissipated in the resistance during the charging of the capacitor ; (iii) the energy supplied by the battery in charging the capacitor. 2×3

(b) What do you mean by the time constant of the circuit ? 2

11. (a) Derive expressions for voltage gain and the input impedance of an inverting amplifier using an OP AMP.

$2\frac{1}{2}+2\frac{1}{2}$

(b) Draw the circuit of voltage-to-current converter using OP AMP and explain its operation.

$1\frac{1}{2}+2\frac{1}{2}$

Group—C

Answer any *five* questions. 5×4

12. What is percentage voltage regulation? Show that for both half-wave and full-wave rectifiers, the percentage voltage regulation = $(R_f/R_L) \times 100\%$, where R_f is the forward resistance of a diode and R_L is the load resistance.

$1\frac{1}{2}+2\frac{1}{2}$

13. Define α and β for a transistor and obtain a relationship between them. 2+2

14. Explain different losses and leakages of a transformer. 4

15. In the circuit of Fig. 2, the switch K_2 is open and the switch K_1 is closed at time t = 0. At time $t = t_0$, the switch K_1 is open and the switch K_2 is simultaneously closed. Sketch the variation of the inductor current i as a function of time. 4

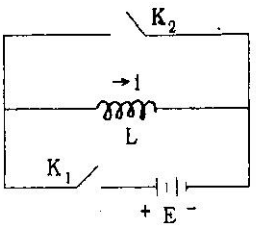

Fig. 2

16. What is the desired position of the Q-point for a minimum distortion and why? Mention the factors that affect the bias stability of a transistor. 2+2

17. Reduce the network of Fig. 3 to an equivalent T network with proper explanation. 4

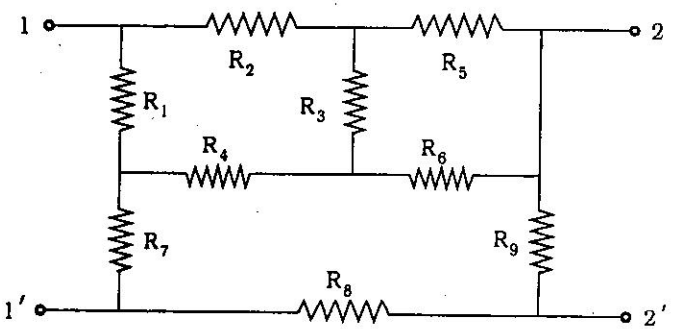

Fig. 3

18. The frequency of a Hartley oscillator is to vary from 60 – 120 KHz. The tuning capacitor can be changed from 100 – 400 pF. The transistor employed in the circuit has $h_{fe} = 90$ and Δ_{re} (i.e. $h_{ie}h_{oe} - h_{fe}h_{re}$) = 0·2 . Find the values of the inductances, neglecting the mutual inductance between them. 2+2

19. Explain the use of OP-AMP as a differentiator. 4

[Internal Assessment — 10]