2016

OLD

Part II 3-Tier

ELECTRONICS

PAPER—II

(General)

Full Marks : 100

Time : 3 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Group—A

Answer any *two* questions. 15×2

1. (a) What do you mean by positive and negative logic systems ? Explain the significance of the term 'logic'.

(b) Draw a circuit showing how an inverter with an active high input and an active low output turns on an LED during its active condition. Repeat the problem with an inverter with active-low input and an active-high output.

(c) Convert : (i) $(75{\cdot}4375)_{10}$ into binary.

(ii) $(0{\cdot}OAAA055)_{16}$ into decimal.

(3+2)+(3+3)+(2+2)

2. (a) Find out the reduced SOP and POS form of the function F whose output is described by the following truth table.

X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(b) Redesign the circuit in Fig. 1 using (i) all NAND gates, (ii) all NOR gates.

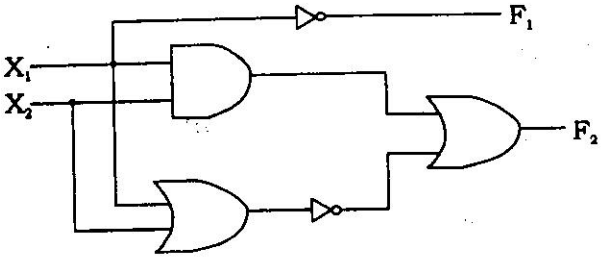

Figure 1

(c) Draw a diagram for optical implementation of AND operation. $(2\frac{1}{2}+2\frac{1}{2})+(4+4)+2$

3. (a) Figure out the main quantity determining the regulation characteristic. Define percentage voltage regulation.

(b) Enumerate different types of filters used at the output of a rectifier. Explain their functions.

(c) Draw the circuit diagram of a series voltage regulator and explain its principle of operation.

$(1+2)+(2+3)+(3+4)$

Group—B

Answer any *five* questions : 5×8

4. Given $A = \bar{B}.C + B.\bar{C}$, then show that

   (i) $A = B.C + \bar{B}.\bar{C}$

   (ii) $B = \bar{A}.C + A.\bar{C}$

   (iii) $C = \bar{A}.B + A.\bar{B}$ 2+3+3

5. (a) Draw block diagram and functional table of a 8 to 1 MUX.

   (b) Cascade two 4-to-1 MUX IC chips to make an equivalent 8-to-1 MUX. (2+3)+3

6. (a) Draw the circuit of a clocked RS flip-flop and explain its operation.

   (b) Explain the use of preset and clear inputs in a flip-flop. $(2+3)+(1\frac{1}{2}+1\frac{1}{2})$

7. Draw the logic circuit of a MOD-10 counter and explain its working with a timing diagram. 3+5

8. It is desired to measure the voltage across the 50KΩ resistor in the circuit of Fig.2. Two voltmeters are available for this measurement : voltmeter 1 with a sensitivity of 1,000 Ω / V and voltmeter 2 with a sensitivity of 20,000 Ω / V. Both meters are used on their 50V range. Calculate : (i) The reading of each meter, (ii) the error in each reading, expressed as a percentage of the true value.

$(2\frac{1}{2}\times 2)+1\frac{1}{2}\times 2$

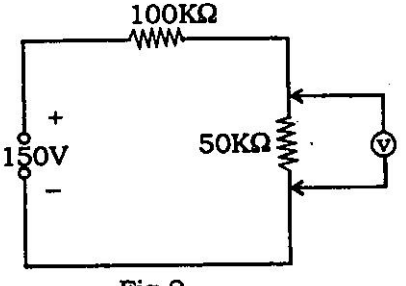

Fig-2

9. (a) Why and how does the condition of balance in an ac bridge differ from that in a dc bridge ?

(b) Find the condition of balance in a generalized AC bridge. 3+5

10. (a) Draw the circuit diagram of an astable multivibrator and explain its principles of action showing collector voltage waveforms.

    (b) What will be conditions to produce square wave and pulse wave by an astable Multivibrator ?

    (2+4)+(1+1)

11. (a) Draw the block diagram of a general purpose CRO indicating its basic components.

    (b) How can the phase difference between two voltages be measures by a CRO ? 4+4

Group—C

Answer any *five* questions : 5×4

12. State De Morgan's theorems and reduce the following function using that.

$$X = \overline{\left(\overline{A + B + \bar{C}}\right)\left(\overline{\overline{AB} + \overline{CD}}\right) + \overline{BCD}}$$ 2+2

13. Explain a basic 2-input TTL NAND gate circuit. 4

14. Give the truth table of a full adder and hence show that a full adder can be constructed using two half adders and an OR gate. 2+2

15. What is a D-type flip-flop? How can a JK flip-flop be converted into D flip-flop? 2+2

16. What is a Q meter? Draw a basic Q meter circuit. 2+2

17. The symmetrical square wave voltage of Fig.3 is applied to an average responding ac Voltmeter with a scale calibrated in terms of the rms value of a sine wave. Calculate : (i) the form factor of the square wave voltage, (ii) the error in the meter indication.

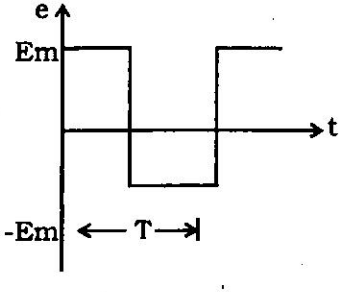

Fig.3

18. Explain the term 'sweep voltage' in connection with a CRO. What are the advantages of dual trace over dual beam for multiple trace oscilloscope ? 2+2

19. Draw the basic block diagram of a frequency counter. A frequency counter capable of measuring an unknown frequency to within $1H_z$ by measuring frequency rather than period world require what minimum gate time ? 2+2

[Internal Assessment – 10]