2017

MCA

1st Semester Examination

BASIC ELECTRONICS & DIGITAL LAB.

PAPER—MCA-107

(Practical)

Full Marks : 100

Time : 3 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any one question.   1×70

(Lottery basis)

1. Design XOR and XNOR gates using minimum number of NAND gates.

2. Design XOR and XNOR gates using minimum number of NOR gates.

3. Design a 4 bit odd parity generator circuit.

(Turn Over)

4. Design a 4 bit even parity generator circuit.

5. Design a full adder using NAND gates.

6. Design a full subtractor using NAND gates.

7. Design a clocked SR flip-flop using NAND gates.

8. Design a J–K master slave flip-flop using NAND gates.

9. Design a circuit to convert BCD to Excess 3 code.

10. Design a 4 bit ripple counter.

11. Design a 3 to 8 line decoder using basic gates.

12. Design a full adder using 8 : 1 MUX.

13. Design a 4 bit adder using 7483.

14. Implement the following using 8 : 1 MUX

   F(A, B, C, D) = (0, 2, 4, 6).

15. Design a circuit to convert Gray code to Binary number.

[Practical Note Book : 10 Marks]

[Viva-Voce : 20 Marks]

——