2017

M.Sc. 4th Semester Examination

ELECTRONICS

PAPER—ELC-404

Full Marks : 50

Time : 2 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(VLSI Technology)

Answer Q. No. *1* and any *three* from the rest.

1. (a) What do you understand by 'a class 100 clean room' ?

(b) Differentiate between positive photoresist and negative photoresist in VLSI Technology.

(c) What do you mean by CMOS Latch up ?

(d) Compare between CMOS technology and BiCMOS Technology.

(e) What do you mean by the λ-based design rules for the layout of VLSI circuit ? 2×5

2. (a) Describe an ion implantation system with a schematic diagram.

(b) What are the problems entangles in ion implantation ? How the problem can be solved ?

(c) Mention SIMOX process and its uses.

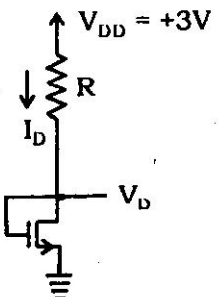
3+(2+2)+(2+1)

3. (a) Write down the NMOS fabrication process with suitable diagrams.

(b) What do you mean by short channel effects ? Briefly discuss about them.

(c) Why constant voltage scaling is preferred in VLSI Technology ? 5+3+2

4. (a) Design the circuit in fig. below to obtain a current I_D of 80 μA. Find the value required for R and find the dc voltage V_D. Let the NMOS transistor have V_t = 0.6V, $\mu_n COX$ = 200 $\mu A/V^2$, L = 0.8 μm and W = 4 μm. Neglect the channel-length modulation effect.
(i.e., assume $\lambda = 0$)



(b) Briefly discuss epitaxial deposition technique.

(c) Differentiate between wet etching and dry etching.

(2+2)+5+1

5. (a) Draw the schematic diagram of a three-phase CCD with overlapping gate electrodes. Explain its operation with potential energy and charge distributions.

(b) Draw a cross-sectional view of a buried channel CCD (BCCD). Explain the importance of BCCD.

(3+4)+(2+1)

6. (a) Define Rent's Law. Estimate the number of gates that can be included on a logic-gate array chip which in to be assembled in a 100 I/O package. Assume $\alpha = 4.5$ and $\beta = 0.5$.

(b) What are the factors associated with packaging ?

(c) Discuss different package design used in VLSI Technology.

(d) What are the different bonding used in VLSI assembly technologies ? (1+3)+2+2+2

[Internal Assessment — 10 marks]

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