2017

M.Sc. 2nd Semester Examination

ELECTRONICS

PAPER—ELC-205

(Practical)

Full Marks : 50

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(Digital Electronics Lab.)

Answer *one* question selecting it by a lucky draw.

1. Design half adder and full adder circuit using NAND gates only.

2. Design half adder and full adder circuit using MUX only.

3. Design half subtractor and full substractor circuit using NAND gates only.

4. Design half substractor and full substractor circuit using MUX only.

5. Design 4-bit comparator circuit.

6. Design a circuit to convert a BCD to gray code and gray to BCD code.

7. Design a JK and MS flip-flop and realize its truth table.

8. Construct a MOD-10 synchronus counter.

9. Design a BCD synchronus counter.

10. Design a BCD ripple counter.

11. Design a random counter which will count following states :
(0, 3, 5, 4, 2, 6, 8, 7, 1)

12. Design a astable multivibrator using 555 timer with duty cycle. Duty cycle to be provided in the exam hall.

13. Design a R-2R ladder D/A converter.

Distribution of Marks

Theory	:	10 Marks
Circuit (Implementation)	:	10 Marks
Experiment	:	05 Marks
Results and discussion	:	10 Marks
Viva-voce	:	10 Marks
Lab. Note Book	:	05 Marks
Total	:	50 Marks