2017

M.Sc. 2nd Semester Examination

ELECTRONICS

PAPER—ELC-203

Full Marks : 50

Time : 2 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(Digital Electronics and Mobile Communication)

Answer Q. No. *1* and any *three* from the rest.

1. (a) What are the drawbacks of ECL logic families ?

(b) A binary ripple counter is required to count up to 16383_{10}. How many flip-flops are required ?

(c) What is the advantage of R-2R ladder type DAC converter over weighted resister DAC ?

(d) Draw the circuit of 3-input CMOS NAND gate.

(e) What do you mean by ISDN in digital communication ?

2×5

2. (a) What is a race around condition ? How it can be avoided ?

(b) Convert JK F/F to D F/F. (2+3)+5

3. (a) Design a type T counter that goes through states 0, 3, 5, 6, 0 ....

(b) Differentiate between synchronous counter and asynchronous counter.

(c) What are the different types of shift register ? Briefly explain about them. 4+2+(1+3)

4. (a) Design Half adder logic circuit using CMOS logic.

(b) Explain totempole arrangement in TTL logic family.

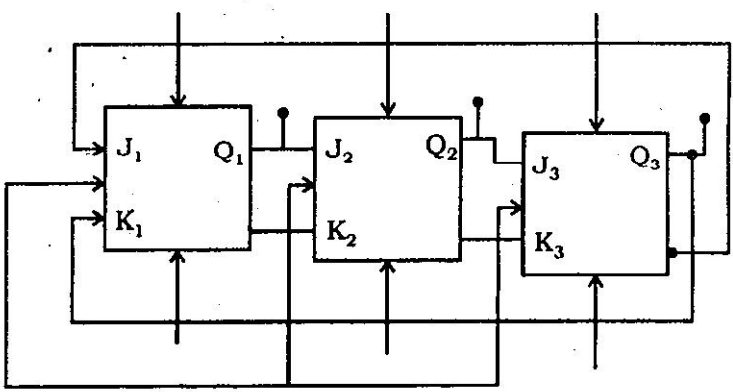
(c) Design 4-bit odd parity generator circuit.

3+4+3

5. (a) Design a monostable multivibrator circuit with 555 timer.

(b) With reat circuit diagram describe the function of R-2R ladder type D/A converter. If the full scale deflection of a 4 bit D/A converter is 8 V then what is the output value at 1100 ?

(c) Find out the different output state for the following circuit :



3+4+3

6. (a) What is network topology ? Explain with two different such topology ?

(b) Describe briefly the idea of packet switching network.

(c) Explain the reuse of frequency in 'cell' concept of mobile communication. With block diagram briefly demonstrate the signal transmission and reception in mobile communication. 3+3+4

[Internal Assessment — 10 marks]

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