2017

M.Sc.

3rd Semester Examination

ELECTRONICS

PAPER—ELC-303

Full Marks : 50

Time : 2 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(VLSI Engineering)

Answer Q. No. *1* and any *three* questions from the rest.

2×5

1. (a) Write down the steps for VLSI design flow :

   (b) 'Class 1000', 'Class 100' and 'class 10' – amongst the three clean rooms which one will you prefer for a lithographic process and why ?

(c) What is extrinsic diffusion ?

(d) Why do we scale MOS transistor ?

(e) What do you understand by the functional yield and parametric yield ?

2. (a) Describe with a diagram the various charges associated with thermally oxidized silicon.

(b) What is the bird's beak structure in the oxidation proces ? How is it prevented ?

(c) If a silicon oxide of thickness x is grown by termal oxidation, what is the thickness of silicon being consumed ? The molecular weight of Si is 28.9 g mol^{-1}, and the density of Si is 2.33 g cm^{-3}. The corresponding values for SiO_2 are 60.08 g mol^{-1} and 2.21 g cm^{-3}.

4+(2+1)+3

3. (a) Mention the features that must be considered in metallization scheme in VLSI.

(b) Explain the problems arising from aluminium deposition. How can these problems be minimized ?

(c) *Estimate the intrinsic* RC value of pro parallel Al wires 0.5 μm×0.5 μm in cross section, 1 mm in length, and seperated by a polymide (R ~ 2.7) dielectric layer that is 0.5 μm thick. The resistivity of Al is 2.7 μm – cm.

2+(2½+2½)+3

4. (a) What is CMOS latchup ? How is it prevented ?

(b) Write down the advantages of retrograde well over conventional well.

(c) Explain gate-engineering technology in the fabrication of CMOS devices. (2½+2½)+2+3

5. (a) What is Enter-path method for layout in VLSI design ?

(b) Consider the logic function $g = \overline{a.b.c + d}$. Find the Euler path. Use it to draw a stick level layout.

(c) Draw the layout for CMOS NAND gate. 2+(2+3)+3

6. (a) Explain the different criteria to be fulfilled for a good package design in VLSI technology. Mention different levels of packaging.

(b) Describe the steps followed to design a differential CMOS amplifier.

[Internal Assessment : *10 Marks*]
