2016

M.Sc.

4th Semester Examination

ELECTRONICS

PAPER—ELC-404

Full Marks : 50

Time : 2 hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(VLSI Technology)

Answer *Q. No. 1* and any *three* from the rest.

1. (a) RF sputtex and thermal evaporator— both are thin filer depositors. Point out the difference of materials can be deposited using these equipment.

(b) What is proximity effect in e-beam lithography ?

(c) Explain design rules for the layout of VLSI circuits.

(d) Describe Rent's rule.

(e) What is a buried-channel CCD ? 2×5

2. (a) How metal ions can be reduced in grown silicon dioxide ?

(b) A 2000 Å gate oxide is required for some technology. Dry oxidation will be carried out at 1000°C. Find out the time required for oxidation.

Assume : → there is no initial oxide.

° → $A = 0{\cdot}165\,\mu m$, $B = 0{\cdot}0117\ \mu m^2/hr$ at 1000°C.

B/A is known as linear rate of co-efficient

B is known as parabolic rate of co-efficient.

(c) State the purpose of replacing SiO_2 with a high K dielectric in short channel MOSFET.

(d) State the advantages and disadvantages of using metal gate (instead of poly gate in short channel MOSFET. $2+3+2\frac{1}{2}+2\frac{1}{2}$

3. (a) What are the factor to be taken care for metallization in VLSI ?

(b) Describe sputtering technique for metal film deposition.

(c) Explain damascene technology.

If we replace Al with Cu wire associated with some low-R dielectric (R = 2·6) instead of a SiO_2 layer, what percentage of reduction in the RC time constant will be achieved ? The resistivity of Al in 2·7 $\mu\Omega - cm$ and the resistivity of Cu is 1·7 $\mu\Omega - cm$

2+3+(3+2)

4. (a) Describe with neat diagrams the steps followed in the fabrication of an n-channel depletion MOSFET.

(b) What do you mean by a long-channel MOSFET and a short channel MOSFET ?

(c) Mention the advantages of developing BiCMOS technology. 6+(1+1)+2

5. (a) Why do we scale MOS transistor ? Describe the sealing methods used in VLSI design.

(b) A microprocessor consumes 0·4 mW/MH_3 when fabricated using 180 nm process. With typical standard gates, the area of the processor is 0·7 mm^2. Assume a 100 MH_3 clock frequency, and 1·8 V power supply.

Using fixed voltage sealing and constant frequency, what will the area, power consumption of the same processer be, if scaled to 120 mm technology, assuming the same clock frequency.

(c) What is a thin-film transistor ? (3+3)+(1+1)+2

6. (a) What do you mean by different levels of packaging ?

(b) Describe chip-to-package interconnection methods used in VLSI technology.

(c) Suppose an IC manufacturer wants to establish a defect density chart. Twenty different samples of size n=5 wafers are inspected, and a total of 183 defects are found. Set up the defect density chart for this situation.

2+5+3

Internal Assessment — 10