2016

M.Sc.

3rd Semester Examination

ELECTRONICS

PAPER—ELC-301

Full Marks : 50

Time : 2 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(Microprocessor and its Applications)

Answer Q. No. *1* and any *three* questions from the rest.

1. (a) What are the advantages of segmented memory ?

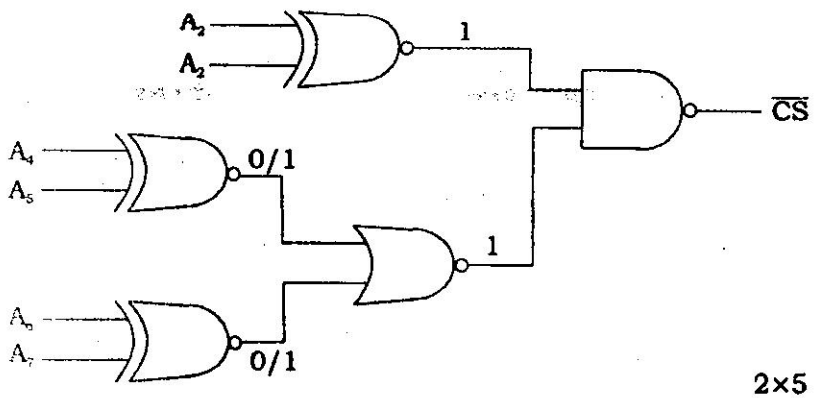
(b) Indicate different machine cycles with status and control signals for 8085 μp.

(c) Explain the instruction RDEL.

(d) Identify the register contents and flags as the following instructions are being executed

	A	S	Z	CY
MVI A, 7H				
ORA A				
RAR				
RAL				

(e) The decoding circuit shown in figure below has been used to generate the active low chip select signal ($\overline{CS}$) for a microprocessor peripheral (the address lines are designed as A_0 to A_7 for input addresses). Determine the input address for $\overline{CS}$.



2×5

2. (a) What do you mean by pipelined architecture ? How is it implemented in 8086 μp ?

(b) Draw and discuss a typical minimum mode 8086 μp system. (2+2)+(3+3)

3. (a) Draw the interrupt circuit diagram for 8085 μp and explain.

(b) In an interrupt driven system EI instruction should be incorporated at the beginning of the program. Why ? (3+4)+3

4. (a) Write a subroutine to set the zero flag and check whether the instruction JZ functions properly, without modifying any register contents other than flags.

(b) Explain a loop within a loop technique for a time delay. Calculate the delay in the following loop, assuming the system clock period is 0.33 μs.

Label	Mnemonics	8085 mp T-states	
	LXI B, 12FFH	10	
LOOP :	DCX B	6	
	XTHL	16	
	XTHL	16	
	NOP	4	
	NOP	4	
	MOV A, C	4	
	ORA B	4	
	JNZ LOOP	10/7	4+(3+3)

5. Explain the modes of serial communication supported by 8251. With a sketch explain receiver section. 7+3

6. (a) Compare synchronous and asynchronous serial transmission. Draw the serial bit format for ASCII character I (49H) at 1200 band.

   (b) Explain IEEE-488 interface standard. What is meant by current loop interface ? Mention its advantages.

(2+2)+(3+2+1)

(Internal Assessment : 10 Marks)