

2016

M.Sc. 1st Semester Examination

COMPUTER SCIENCE

PAPER—COS-102

Full Marks : 50

Time : 2 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(Advanced Computer Architecture)

Answer any four questions.

1. (a) What is arithmetic pipeline ?
- (b) Implement floating point adder-subtractor using four stage pipeline.
- (c) Calculate $0.9504 \times 10^3 + 0.8200 \times 10^2$ using the implemented arithmetic pipeline. 2+5+3

(Turn Over)

2. Consider the reservation table of a three stage pipeline processor.

→ time

	1	2	3	4	5	6
S_1	x				x	
Stage S_2			x			
S_3		x		x		x

- List forbidden and non-forbidden latencies.
- Construct collision vector.
- Draw state diagram.
- List all simple and greedy cycles.
- Calculate MAL.

2+4+3+1

3. (a) Consider a n level memory hierarchy and h_i is the hit ratio of module M_i , $0 \leq i \leq n - 1$. Find out the access frequency and effective access time.

(b) What is coherence property of memory hierarchy? Explain the techniques to maintain the property.

3+3+4

4. (a) Explain snoopy protocol of multiprocessor.

(b) Draw and explain NUMA model of multiprocessor.

(c) Distinguish COMA and UMA model of multiprocessor.

3+4+3

5. (a) Explain structural hazard with an example.

(b) Find out the maximum speed up ratio of a k stage pipeline.

(c) Consider a 4 stage pipeline processor with clock rate 20 MHz and number of instruction 4000. Calculate the speed up, efficiency and through put.

2+3+5

6. Answer any *four* questions :

- (a) Data Hazard ;
- (b) CISC ;
- (c) Clock skewing ;
- (d) Carry propagate adder ;
- (e) Locality of reference ;
- (f) Virtual Memory.

$2\frac{1}{2} \times 4$

Internal Assessment — 10
