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Electrical and Chemical Characteristics of Ta_2O_5 Gate Dielectrics on Ge-rich SiGe Heterolayers

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ABSTRACT

The charge trapping/detrapping behavior in ultra-thin tantalum pentoxide oxide (Ta_2O_5, equivalent oxide thickness ~1.76 nm) is presented under constant current stressing (CCS, 0.255 to 1.02 C. cm^{-2}). The Ta_2O_5 film have been deposited on Ge-rich SiGe (Ge~85%) heterolayers using tantalum pentaethoxide [$Ta(OC_2H_5)_5$] as an organometallic source at low temperature (~150 °C) by plasma enhanced chemical vapor deposition (PECVD) technique. The surface chemical states of Ta_2O_5 film has been analyzed by X-ray photo electron spectroscopy (XPS). Fixed oxide charge density (Q_f/q) have been studied in constant current stressing.

Keywords: Constant Current Stressing, Ge-rich SiGe, High-k dielectrics (Ta_2O_5) and XPS.

1. Introduction

Complementary metal-oxide-semiconductor (CMOS) technology has received a lot of attention due to its advantages in VLSI circuit. As performance limits due to SiGe CMOS downscaling are approached, Ge-rich SiGe/SiGe heterostructure layers promise a new direction for innovation in SiGe technology [1]. Thin layers of insulating high-k materials are currently being considered as a replacement for SiO_2. Ta_2O_5 has been suggested as a possible alternative gate dielectric for 45 nm technology node [2, 3]. The present study we have adopted Ta_2O_5 as a promising alternative high-k material. The band gap of Ta_2O_5 is about 4.5 eV for amorphous films. The calculated conduction band offsets for Ta_2O_5 on silicon are 1.5 eV. Ta_2O_5 has a dielectric constant of 25 in thin film form, which is high enough to achieve lower effective oxide thickness (EOT) [4, 5]. However, many challenges have to be met while integrating high-k gate dielectric with Ge-rich SiGe for use as channel in future CMOS technologies. In fact, understanding on the integration of high-k dielectrics and metal gate electrodes with Ge-rich SiGe need further investigations.

In this paper, we report on the reliability properties of μ-wave plasma deposited high-k gate dielectric (Ta_2O_5) films on Ge-rich SiGe heterolayers. The

composition and chemical states in Ta_2O_5 thin film analyzed using XPS. Charge trapping characteristics of Ta_2O_5 film was studied by applying constant current stresses. The fixed oxide charge density (Q_f/q) with injected fluences (N_{inj}) has been studied in detail.

2. Experimental

The Ge-rich (Ge ~ 85%) SiGe layer (~ 0.15-0.2 μm thick) was deposited on the SiGe relaxed buffer layer which was gown on n-type Si (100) with resistivity 10-20 Ω-cm [6]. The samples were subjected to a standard cleaning schedule followed by dipping in a dilute 1% HF solution and were chemically etched in H_2O_2: H_2SO_4 to remove the native oxide layers from the substrate just before loading into the chamber. Tantalum pentaethoxide [$Ta(OC_2H_5)_5$] were used as the organometallic sources for the deposition of Ta_2O_5 films on Ge-rich SiGe layer using PECVD in a microwave (700 W, 2.45 GHz) plasma cavity (0.37×0.37×0.26 m^3) discharge system at 550 mTorr for 45s. The film thickness was estimated to be ~11.3 nm (EOT ~1.76 nm) by a single wavelength ellipsometer (Gaertner L-117). For the electrical measurements, MOS capacitors were fabricated on Ta_2O_5 films by evaporating circular Al dots (area: 1.96×10^{-3} cm^2, thickness: 150-200 nm) through a shadow mask. Current-Voltage (I-V) and Capacitance-Voltage(C-V) measured by applying constant current stresses.

3. Chemical Characterization

XPS was used to analyze the composition and chemical states in Ta_2O_5 film and its interface with $Si_{0.15}Ge_{0.85}$. The photoelectrons were separated by a concentric hemispherical analyzer with a pass energy of 50 eV and an instrumental resolution of 0.6 eV measured as the full width at half maximum (FWHM) of the Ag $3d_{5/2}$ photoelectron peak. The binding energies E_b have been corrected for sample charging effect with reference to the C 1s line at 284.5 eV for the surface of the oxide. Figure 1 (a and b) illustrates the Ta 4f and O 1s photoelectron spectra of the as-grown film. The solid line represents the as-recorded data. The Ta 4f signal (figure 1a) is fitted with two peaks located at 27.1 eV (FWHM 1.24 eV) and 29.07 eV (FWHM 1.29 eV) and energy separation of 1.97 eV and area ratio of 1.08, which are representative for Ta $4f_{7/2}$ to Ta $4f_{5/2}$ spin orbital splitting. The energy position of these peaks is close to the binding energy of Ta in stoichiometric Ta_2O_5 [7].

The Ta 4f spectrum shows no peak at lower energy side of the main peak, i.e., there is no characteristic of metallic Ta. These results suggest that the film at the surface is very close to the stoichiometric Ta_2O_5 with a negligible amount of non-oxidized Ta. The O1s spectra at the surface of the samples can actually be fitted with two Gaussian components (figure 1b). The position of the O1s main peak at 530.70 eV (FWHM = 2.07 eV) and small peak located at 532.72 eV (FWHM = 1.45 eV) is usually attributed to surface contamination [8]. The line at about 532 eV is really the expected position characteristic of SiO_2 but the line at 532.72 eV is suggested that

the sub-oxide of Si is presence [9]. The lower binding energy line referred as Ta_{1s}^{Ta-O} at 530.70 eV is from Ta-O bonding [10].

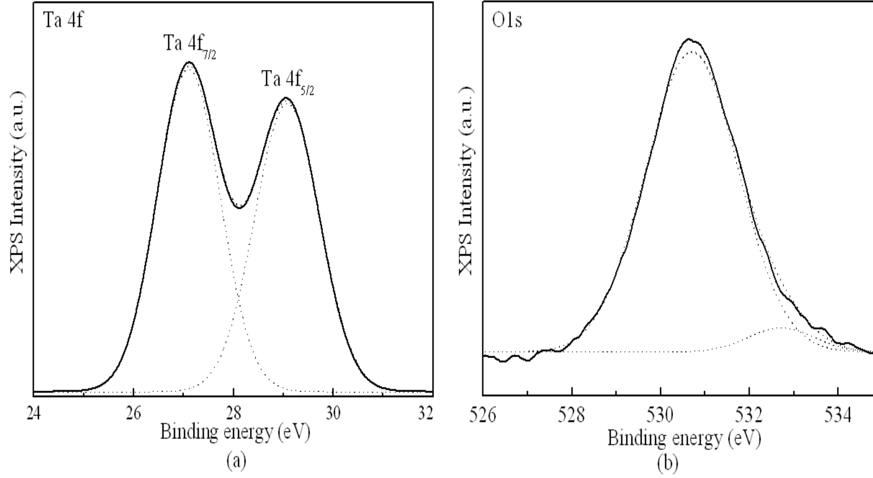

Figure 1: Ta 4f: (a) and O 1s (b) photoelectron spectra at the surface of as-grown Ta_2O_5 films (solid lines). Both spectra are decomposed into two bonding states (dotted line).

4. **Electrical Characterization**

The traps in insulators are extremely important, since the presence of the oxide traps significantly affects the MOSFET device performance. Thus, the origin of oxide traps should be clearly understood in order to control the oxide traps. In the following, a comparison of charge trapping behavior of the samples, studied by continuously monitoring the change in gate voltage (ΔVg) required to maintain a constant current (20 $mA.cm^{-2}$) under gate injection, is shown in figure 2.

The positive shift of ΔVg indicated mainly electrons are trapped inside the tantalum pentoxide. In fact, the oxygen vacancy and oxygen interstitial are the two most likely intrinsic point defects in Ta_2O_5 due to possible multiple valence of Ta. Moreover, the number and spatial distribution of defects in each charge state depend on the method of their creation, presence of the electron source, applied voltage and temperature. In order to model the experimentally observed ΔVg vs. t curve, electron fluences dependent voltage expressions developed by considering electron trapping kinetics have been used. The trapping kinetics is described by a first-order rate equation [11] as:

$$\frac{dN_t}{dt} = n\vartheta_t \sigma_t (N_{ot} - N_t) \quad (1)$$

where N_t is the filled trap density, N_{ot} is total trap density, n is conduction-band electron density, σ_t is trap capture cross section, and υ_t is thermal velocity of

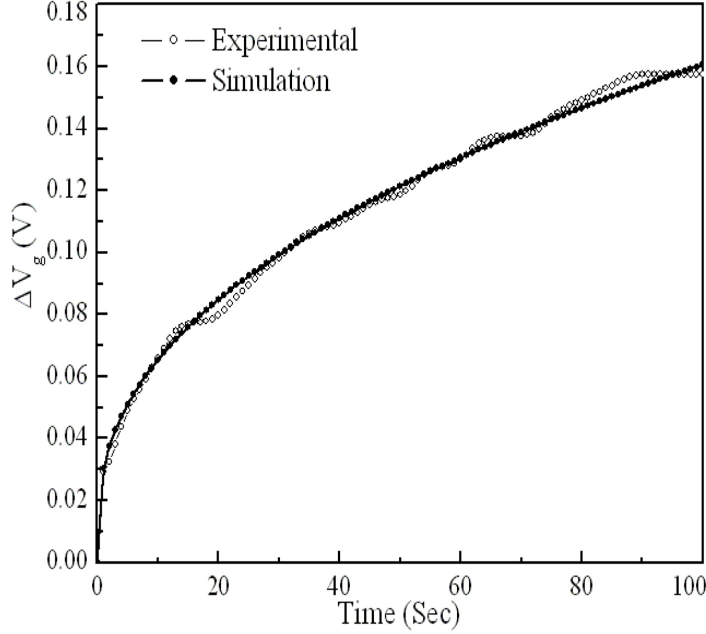

Figure 2: The stress time dependence of increasing gate voltage shift (ΔV_g) observed during constant current stressing at 20 mA cm^{-2} for 100s.

electron. The gate voltage shifts estimate minimizing the surface potential ($\Delta\psi_s$) affect on the capture cross-section measurement and effective trap density is:

$$\Delta V_g = A \sum_i \frac{qN_{ot,i}}{C_{ox}}\left[1 - e^{-\langle\sigma_t\rangle_i N_{inj}}\right] + \beta t^{\delta} \tag{2}$$

where C_{ox} being accumulation capacitance, A is the area of the capacitor, q is the electronic charge, N_{inj} is the injected charge density and $\langle\sigma_t\rangle$ is the average capture cross-section of oxide traps. The second term takes into account the power-law dependent stress-induced voltage shift (SIVS) contributing to gate voltage shift, where β is a constant and δ is a power exponent whose best-fit value is in the range of 0.43 for Ta_2O_5. This simulated result suggests that the traps generated during the electrical stress from neutral centers in Ta_2O_5 layer. The electron traps and the electron trap levels are located at very deep levels below the conduction band edge in case of unstressed film [11]. The constant current stressing generated new shallow trap centers closer to the conduction band and tunnel through the oxide. In trapping characteristics, there are two important parameters, capture cross-section $\langle\sigma_t\rangle$ and trap density (N_{ot}) are determined. Carrier injection usually induces not only capture of injected carriers by dielectric traps but also generates interface states. Now to distinguish traps from one another, assuming that the differences between $\langle\sigma_t\rangle$'s are large enough, the following approximate relation is obtained:

$$ln\left(\frac{\partial \Delta V_g}{\partial N_{inj}}\right) = \sum_i \left[ln\left(\frac{q}{C_{ox}}\langle\sigma_t\rangle_i N_{ot,i}\right) - \langle\sigma_t\rangle_i N_{inj}\right] \quad (3)$$

Thus, as shown in figure 3, a plot of $\ln\left(\partial \Delta V_g / \partial N_{inj}\right)$ *vs.* N_{inj} would provide a straight line with the slope $-\langle\sigma_t\rangle$ and the intersection $\ln\left(qN_{ot}\langle\sigma_t\rangle / C_{ox}\right)$ in the respective region associated with each kind of trap. The extracted capture cross-section and trap density are 8.28 $x10^{-18}$ cm^2 and $1.6x10^{14}$ cm^{-2}, respectively. It may be noticed that the values of σ is smaller compared to ~1.5×10^{-16} cm^2 in SiO_2 which indicates that these traps are coulombic in nature [11].

The effect of constant current stressing (CCS) on leakage current characteristics of Ta_2O_5 with different stress time of 100 s and 200 s is shown in figure 4. It is noticed that the stress induced leakage current (SILC) increases with injected fluences, which is attributed to the generation of localized defects as well as trap states near the injection interface. SILC is defined as the conduction mechanism related to the generation of electron traps within the oxide resulting from electrical stress [11]. The effect of CCS on capacitance–voltage characteristics has been investigated at 1MHz under different stress time, see figure 5. In particular, dispersion is observed at accumulation region. Normally, the measured capacitance in the accumulation region is dependent on oxide/substrate interface properties. The X-ray photoelectron spectroscopy analysis indicated the Si sub-oxide presence at oxide/substrate interface and also small oxygen peak (located at 532.72 eV) was attributed to surface contamination. The accumulation dispersion observed due to the presence of an unwanted lossy dielectric layer in oxide/substrate interface. The positive flat-band voltage, V_{fb} shifts after CCS also show electron trapping in the high-k dielectrics. As explained earlier, the creation of electron traps in high-k gate dielectrics is due to oxygen vacancy.

The fixed oxide charge densities, which are assumed to be located at the insulator/substrate interface, were calculated from the expressions $Q_f / q = \frac{C_{ox}}{Aq}\left(\Phi_{ms} - \Phi_f - V_{fb}\right)$, where Φ_{ms} is the metal-semiconductor work function, Φ_f is the Fermi potential range and V_{fb} is the flat-band voltage of that C–V curve. The fixed oxide charge density decreases from 5.46×10^{12} cm^{-2} to 5.41×10^{12} cm^{-2} after CCS. It may due to the partial compensation of the positive fixed oxide charge by incorporation of negative charge during constant current stressing.

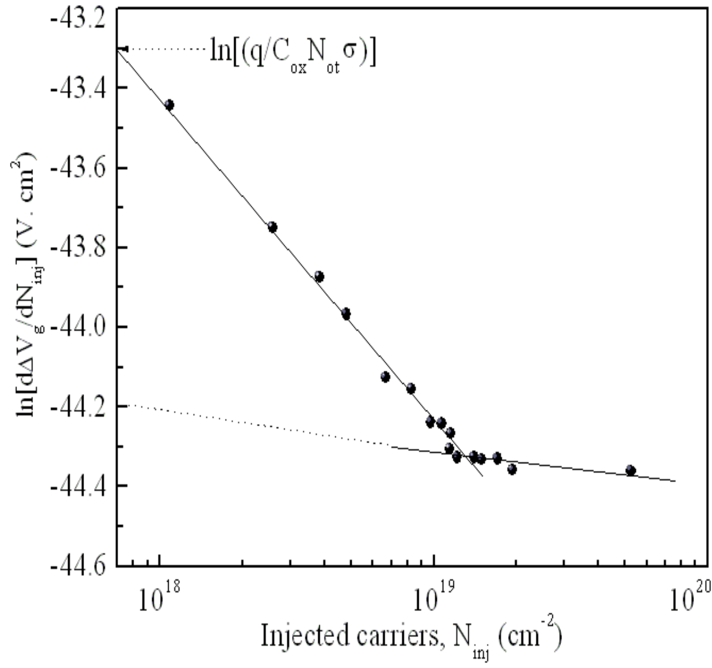

Figure 3: The $\ln\left(\frac{d\Delta V_g}{dN_{inj}}\right)$ vs. N_{inj} plot to determine parameters of the trap density, N_{ot} and capture cross-section, σ_t.

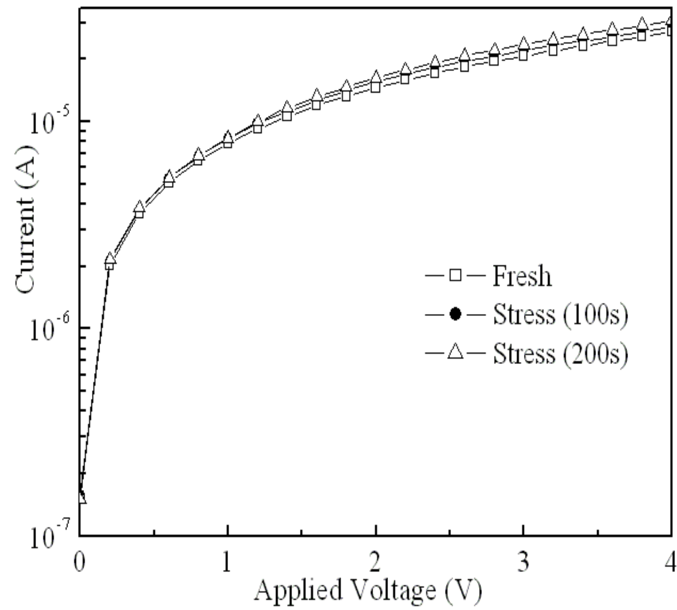

Figure 4: Current–Voltage sweep before and after constant current stressing, SILC is evident across the entire voltage range.

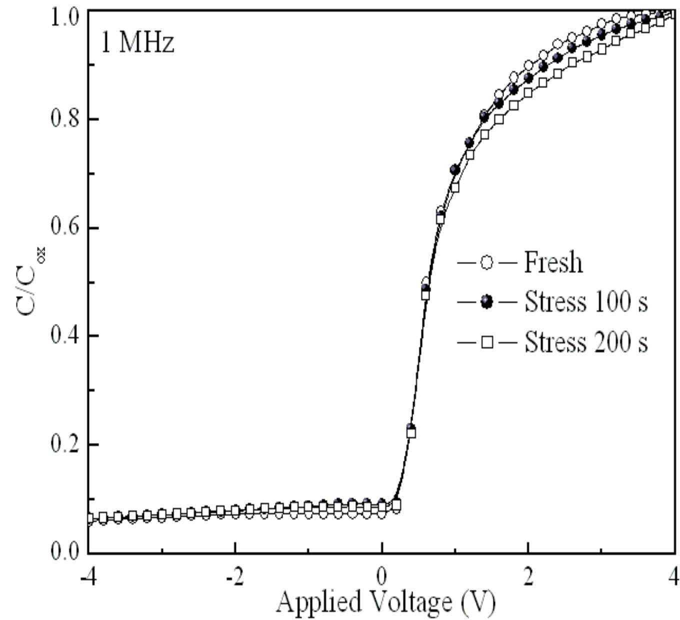

Figure 5: Normalized high frequency (1 MHz) C-V characteristics of Al/Ta_2O_5/Ge-rich SiGe MOS capacitors before and after stressing.

5. Conclusion

In summary, high-k Ta_2O_5 films have been deposited on Ge-rich SiGe heterolayers using microwave plasma deposition technique below 200 ^oC. XPS study revealed that PECVD process favors the generation of thin oxide layer. The capacitance dispersion properties confirm the unwanted lossy layer presence Ta_2O_5/Ge-rich SiGe interface. The charge trapping/detrapping properties of MOS capacitors under stressing in constant current mode have been investigated in detail. However, further improvement in gate oxide (Ta_2O_5) quality and reliability on Ge-rich SiGe layer is needed.

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