Journal of Physical Sciences, Vol. 14, 2010, 247-253
ISSN: 0972-8791, www.vidyasagar.ac.in/journal
Published on December 24, 2010

Low-Voltage CMOS Balanced Output Current Conveyor with Rail-to-Rail Input Stage

Saikat Maiti* and Radha Raman Pal

Department of Physics and Technophysics, Vidyasagar University,
Midnapore-721102, West Bengal, India
*Corresponding author.
E-mail: saikat_physics@yahoo.com, rrpal@mail.vidyasagar.ac.in

Received October 24, 2010; accepted November 25, 2010

ABSTRACT

In this paper, a new CMOS low-voltage balanced output second generation current conveyor (BOCCII) with rail-to-rail input stage is proposed. The rail-to-rail operation can be achieved by placing an n-channel and a p-channel differential input pair connected in parallel. PSpice simulations of the proposed balanced output current conveyor are given using 0.25μm CMOS technology and ±1.2V supply voltage to verify the results. The balanced output current conveyor exhibits a wide dynamic input range and a voltage transfer bandwidth of nearly 31.2MHz.

Keywords: CMOS, balanced output current conveyor (BOCCII), low-voltage, rail-to-rail.

1. Introduction

The second generation current conveyor (CCII) proposed by Sedra and Smith has become a very versatile circuit building block in analog and mixed signal circuit design [1,2]. The CCII is unity gain (current gain) active block exhibiting high linearity, wide dynamic range and high frequency performance where the opamps can not be used, because the opamps are limited by their gain bandwidth product. Some applications where current conveyors have been used include high frequency precision rectifiers, filters, current-mode oscillators, sensors and medical applications, such as electrical impedance tomography (EIT) [3-13].

The CCII has both low and high impedance input port. An ideal CCII has infinite impedance at port Y and zero impedance at port X. The input voltage V_Y applied across Y terminal is conveyed to the voltage V_X across the X terminal. The current at port Z follows the current at port X. The Z terminal is high impedance output port suitable for current output. The direction of the current at port Z relative to that at port X defines whether CCII is positive (CCII+); i.e., ($I_Z=+I_X$) or negative (CCII−); i.e., ($I_Z=-I_X$).

The general representation of the balanced output current conveyor is shown in figure 1. This provides both the positive and negative Z terminal output. The input/output relation could be defined by the following equation [14-15].

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

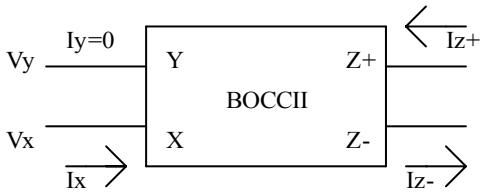

Figure 1 General representation of the BOCCII.

In this paper, a new CMOS low-voltage balanced output current conveyor with rail-to-rail input stage is proposed. This paper is organized as follows. The rail-to-rail input stage is described in section 2. The circuit description of the proposed low-voltage BOCCII is described in section 3. PSpice simulations are presented in section 4 to verify the performance of the proposed BOCCII and some conclusions are drawn in section 5.

2. The Rail-to-Rail Input Stage

The input stage is the key part of a current conveyor. To obtain a large dynamic range, the input common mode voltage should extend from the negative supply rail to the positive supply rail i.e., rail-to-rail [16-17]. This can be achieved by using an n-channel and a p-channel differential pair connected in parallel as shown in figure 2.

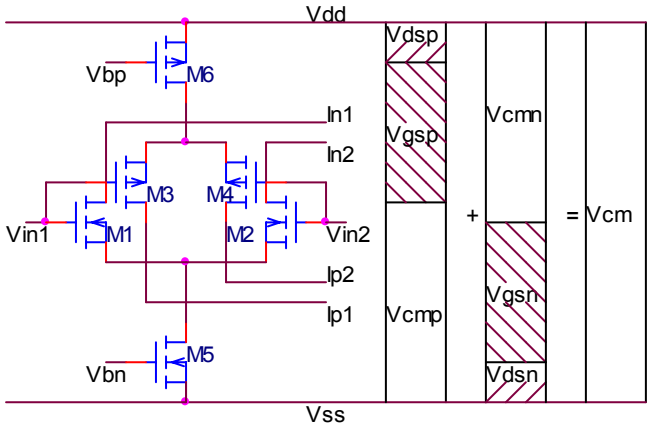

Figure 2 Rail-to-rail input stage with input common mode range.

The input common mode range of a p-channel differential pair is restricted from the negative supply rail voltage to the level of positive rail voltage minus the gate source voltage V_{gsp} of p-channel differential pair and the saturation voltage V_{dsp} of the tail current source. The common mode input range of an n-channel differential pair is restricted from the positive supply rail voltage down to V_{gsn} and V_{dsn} above the negative rail voltage.

When the input voltage at port Y is low only p-channel differential pair (M_3 and M_4) operates, when the input voltage at port Y is high only n-channel differential pair (M_1 and M_2) operates and in the middle range of the input voltage both the differential pairs (M_1, M_2, M_3 and M_4) operate.

3. Circuit Description of the Proposed CMOS BOCCII

The proposed CMOS based BOCCII circuit is shown in figure 3. The structure of the CMOS BOCCII is quite similar to the CMOS CCII in [18]. Here the groups of transistors M_1 and M_2; M_3 and M_4; M_7 and M_8; M_9 and M_{10} as well as M_{13}, M_{14}, M_{17}, M_{19} and M_{21}; and M_{15}, M_{16}, M_{18}, M_{20} and M_{22} are well matched. The current mirrors have a unity gain and all the transistors operate in the saturation region. Here M_5 and M_6 serve as dc current source. The current mirror formed by M_7 and M_8 forces equal currents in the transistors M_1 and M_2. This drives the gate-source voltages V_{GS1} equal to V_{GS2}. Similarly the current mirror formed by M_9 and M_{10} forces equal currents in the transistors M_3 and M_4. This drives the gate-source voltages V_{GS3} equal to V_{GS4}. Thus the voltage at port X follows the voltage at port Y, or $V_X=V_Y$. Transistors M_{11} and M_{12} are connected in the form of source follower, function as current follower stages and provide low output resistance at port X. If $V_Y>0$ and R_X is a resistance connected at port X, the signal current $I_X=(V_Y/R_X)$ will flow out of port X.

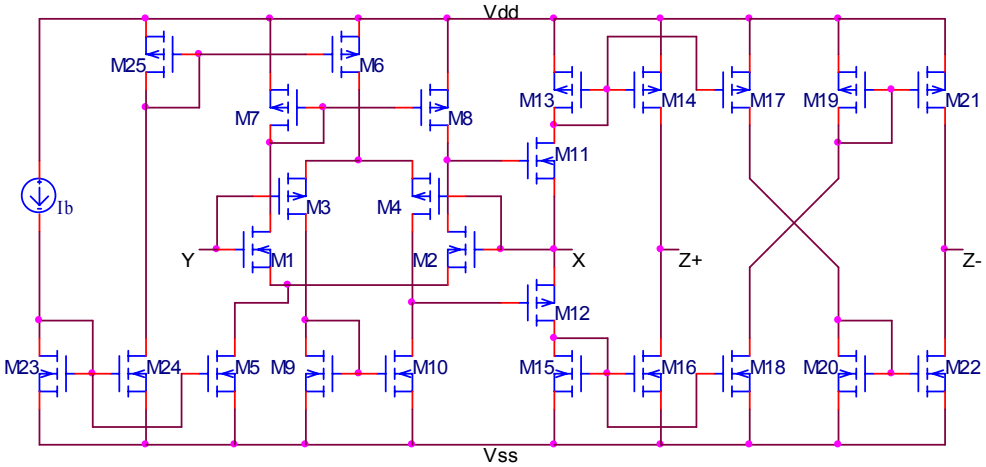

Figure 3 CMOS realization of the proposed low voltage BOCCII.

Now the Z+ terminal output current I_{Z+} is equal to $+I_X$ and flows out of port Z+. It is clearly seen from figure 3 that the current I_{Z+} is in the same direction as the current I_X, i.e., $I_{Z+}=+I_X$. Similarly, the Z− terminal output current I_{Z-} is equal to $-I_X$ and flows in the opposite direction of I_X, i.e., $I_{Z-}=-I_X$.

The output impedance at port Z+ is approximately equal to the output resistance of the current mirror M_{13}-M_{14} in parallel with the output resistance of the transistor M_{16}, and may be expressed as

$$R_{Z+} = \frac{r_{o14} \cdot r_{o16}}{r_{o14} + r_{o16}} \tag{2}$$

Similarly the output impedance at port Z− may be expressed as

$$R_{Z-} = \frac{r_{o21} \cdot r_{o22}}{r_{o21} + r_{o22}} \tag{3}$$

4. Simulation Results

The performance of the proposed low-voltage balanced output current conveyor, as shown in figure 3, have been simulated using level-2 PSpice analog simulation program with 0.25µm CMOS technology. In order to have low power consumption, the supply voltages and the biasing current are decreased down to ±1.2V and 15µA, respectively. In order to reduce the mismatch between transistors, channel lengths are selected as 0.5µm. The aspect ratios of the MOSFETs for the proposed BOCCII is shown in Table I. Voltage transfers of the current conveyor, as shown in figure 4, are determined with high load R_L connected at port X with output ports Z+ and Z− grounded. The frequency response between the port X and port Y is shown in figure 5, where V_Y is the ac-varying signal with 1V magnitude, the X, Z+ and Z– ports terminated with resistances 1kΩ. The bandwidth is around 31.2MHz. The input current transfer for the proposed BOCCII is shown in figure 6 for port Z+ and Z–, respectively. Current transfers are determined with an input current applied on port X. The currents I_{Z+} and I_{Z-} are then the currents that flows through the port Z+ and Z– to the ground and port Y is also grounded. The summary of the simulated results are given in Table II.

Table I: The Proposed BOCCII Transistor Aspect Ratios

Transistors	(W/L) (µm/µm)
M_1, M_2, M_5	21/0.5
M_3, M_4, M_6	48/0.5
M_7, M_8, M_{12}	24/0.5
M_9, M_{10}, M_{11}	10.5/0.5
M_{13}, M_{14}, M_{17}, M_{19}, M_{21}, M_{25}	24/0.5
M_{15}, M_{16}, M_{18}, M_{20}, M_{22}, M_{23}, M_{24}	10.5/0.5

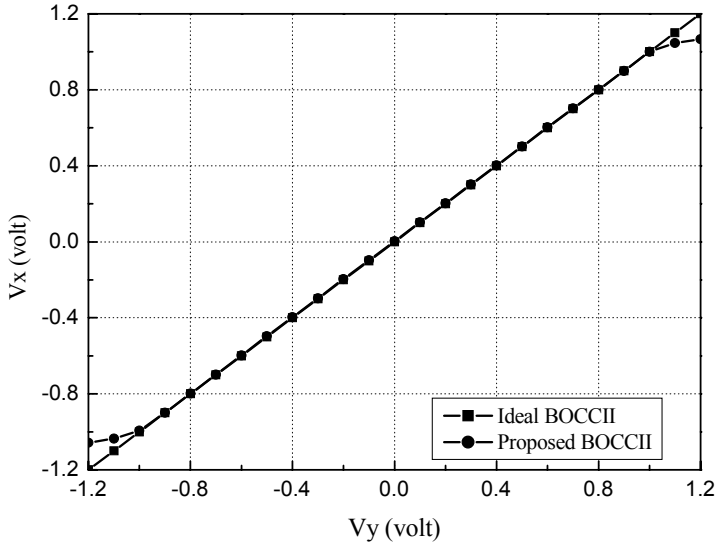

Figure 4 Voltage transfer characteristics from port Y to port X.

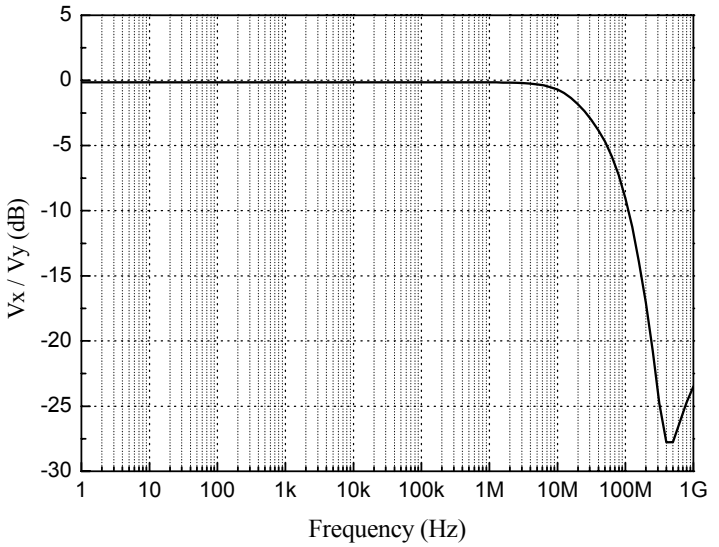

Figure 5 The X terminal frequency response of the proposed BOCCII.

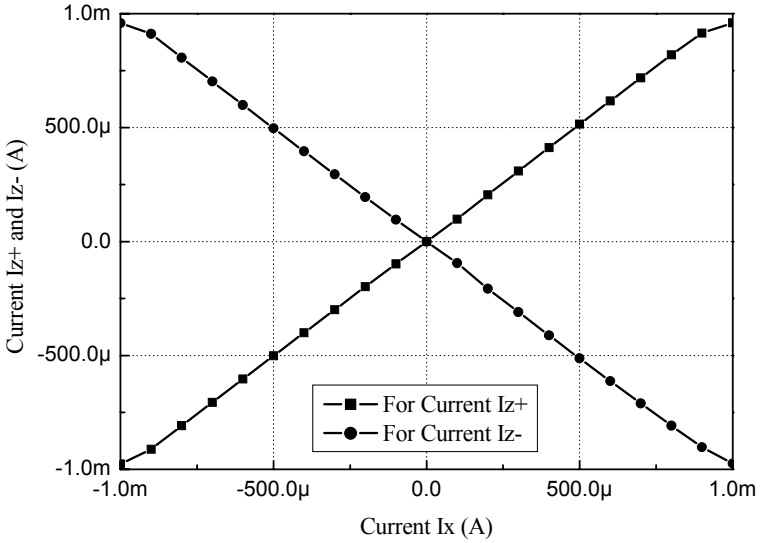

Figure 6 Current transfer characteristics from port X to port Z+ and port Z−.

Table II: PSpice Simulation Results of the Proposed BOCCII.

Parameters	Values
CMOS technology	0.25µm
Power supply	±1.2V
Input voltage dynamic range	Rail-to-rail
Current driving capability (R_X=R_{Z+}=R_{Z-}=1kΩ)	-1mA to +1mA
Current gain	1.0
Voltage gain	0.98
Voltage transfer bandwidth	31.2MHz
Power dissipation	225µW
Output noise	$2.7 nV/\sqrt{Hz}$

5. Conclusion

In this paper, a new low-voltage CMOS BOCCII with rail-to-rail input stage is proposed. The proposed circuit performance has confirmed by using PSpice simulations with 0.25µm CMOS technology and supply voltage ±1.2V. It shows a good overall performance. The most important advantage of the proposed CMOS BOCCII is the increase of the dynamic range.

Acknowledgment

The first author wants to acknowledge UGC, India for providing him junior research fellowship. The authors also acknowledge DST, FIST and UGC-SAP for providing financial support.

REFERENCES

1. K. C. Smith and A. S. Sedra, 1968, *IEEE Proc.*, 56, 1368-1369.
2. A. S. Sedra and K. C. Smith, 1970, *IEEE Trans. Circuit Theory*, CT-17, 132-134.
3. S. R. Djukic, 2008, *Serbian Journal of Electrical Engineering*, 5:2, 263-271.
4. C. L. Hou and C. C. Lin, 2004, *Tamkang Journal of Science and Engineering*, 7:3, 145-148.
5. V. kamil, D. Tomas and C. Josef, 2000, *Radioengineering*, 9:1, 41-44.
6. M. Sagbas, K. Fidanboylu and M. C. Bayram, 2005, *World Academy of Science, Engineering and Technology*, 2, 119-122.
7. S. B. Salem, A. Fakhfakh, M. Loulou, P. Loumeau and N. Masmoudi, 2004, *IEEE*, 0-7803-8656-6/04.
8. D. S. Masmoudi, N. B. E. Fek, S. B. Salem, M. Fakhfakh and M. Loulou, 2005, *Journal of Applied Sciences*, 5:8, 1445-1451.
9. P. Kumar, K. Pal and G. K. Gupta, 2006, *Indian journal of Pure and applied Physics*, 44, 398-401.
10. J. Samitier, M. P. Vidal, S. A. Bota, C. Rubio, S. K. Siskos, T. Laopoulos, 1998, *IEEE Transactions on Instrumentation and Measurement*, 47:3, 708-709.
11. S. Vlassis, S. Siskos and T. Laopoulos, 1999, *IEEE*, 303-308.
12. S. Vlassis and S. Siskos, 2000, *Analog Integrated Circuits and Signal Processing*, 23, 153-162.
13. S. B. Salem, M. Fakhfakh, D. S. Masmoudi, M. Loulou, P. Loumeau and N. Masmoudi, 2006, *Analog Integrated Circuits and signal Processing*, 10470-006-8694-4.
14. A. H. Madian, S. A. Mahmoud and A. M. Soliman, 2005, *IEEE*, 1179-1182.
15. F. Centurelli, M. Diqual, G. Ferri, N. C. Guerrini, G. Scotti and A. Trifiletti, 2005, *Analog Integrated Circuits and signal Processing*, 43, 87-90.
16. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, New York, 2002.
17. G. Ferri and N. C. Guerrini, *Low-Voltage, Low-Power CMOS Current Conveyors*, Kluwer Academic Publishers, 2003.
18. W. Surakampontorn, V. Riewruja, K. Kumwachara and K. Dejhan, 1991, *IEEE Transactions on Instrumentation and Measurement*, 40:4, 699-702.