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Study of Speed Enhancement of a CMOS ring VCO

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ABSTRACT

Positive feedback has been added to a fully differential CMOS amplifier. With the introduction of positive feedback, the delay time reduces and the speed of operation increases. An even or odd number of stages can be cross coupled or directly coupled to form a ring Voltage Controlled Oscillator or Current Controlled Oscillator (VCO/CCO). Pspice simulation shows an improvement (increase) of speed of around 167 %. Instead of using positive feedback if we use negative feedback then also the speed improves but it requires a higher value of feedback resistance, which is not favoured in integrated circuit fabrication. Here the typical supply voltage requirement is ±2 volt. Using this amplifier some applications have also been discussed.

Key words : *Complimentary Metal Oxide Semiconductor (CMOS), Voltage Controlled Oscillator (VCO), Current Controlled Oscillator (CCO), Ring Oscillator, Phase Locked Loop (PLL).*

1. Introduction

Over the last few years there have been rapid increase in chip complexity which has created the need to implement complete analog-digital subsystems on the same integrated circuit using the same technology. For this reason, implementation of analog functions in CMOS technology has become increasingly important [1,2].

This paper presents a high speed low voltage CMOS fully differential amplifier. The circuit features a positive feedback scheme to improve the speed and to reduce the supply voltage requirement of this amplifier Figure 1. Since the circuit is fully differential, push-pull output is possible. To check the improvement in speed an even number of such amplifier stages has been cross coupled to form a ring oscillator Figure 2, whose frequency depends on the delay time of each such amplifier stage. This ring

oscillator also provides a quardrature output which is very much useful in various communication systems.

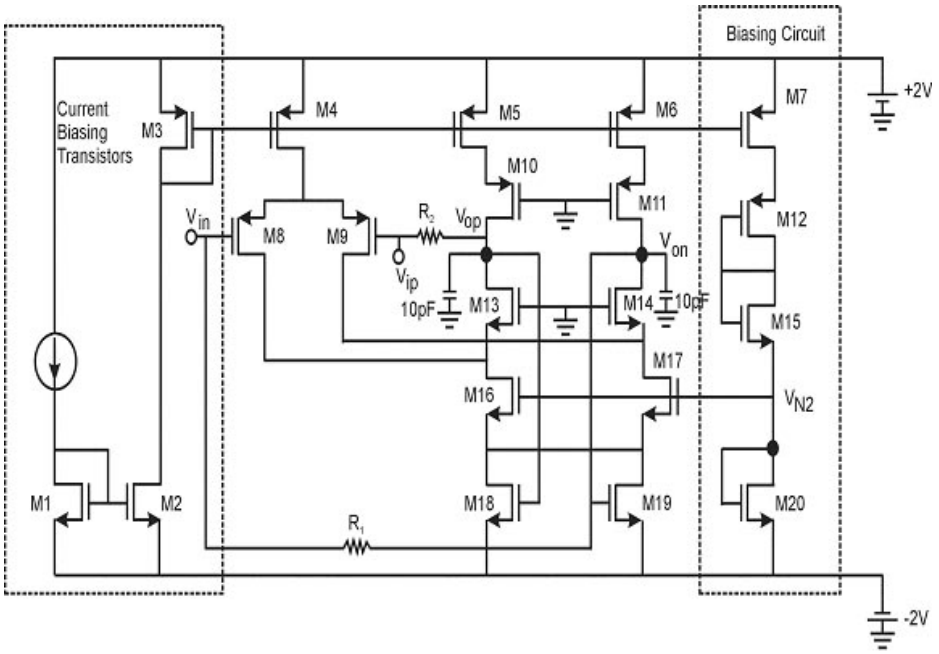

Fig. 1. Circuit diagram of the fully differential CMOS amplifier with positive feedback.

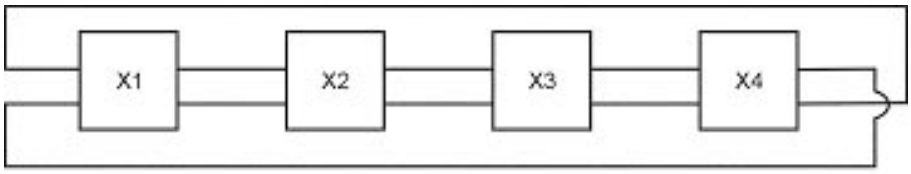

Fig. 2. Block diagram of a 4-stage ring oscillator.

In section 2 gives the operation for decreasing delay time has been discussed. The simulated results of the fully differential CMOS amplifier are discussed in section 3. Section 4 includes come application of this amplifier.

2. Mathematical expression

Figure1 gives the circuit diagram of the fully differential CMOS amplifier using positive feedback scheme. By introducing positive feedback the delay produced by each amplifier stage is reduced and hence the speed of operation increases [3]. The frequency of oscillation depends on the number of the inverter stages, the load capacitances and the current level. It has been tested by connecting 4 number of such amplifier stages in series shown in Figure 2 and the outputs of the last stage are cross coupled with the inputs of the first stage.

2.1 Calculation of phase factor without positive feedback

A simple CMOS operational amplifier with positive feedback is shown in Figure 3. An AC small signal equivalent circuit of Figure 3 is shown in Figure 4.

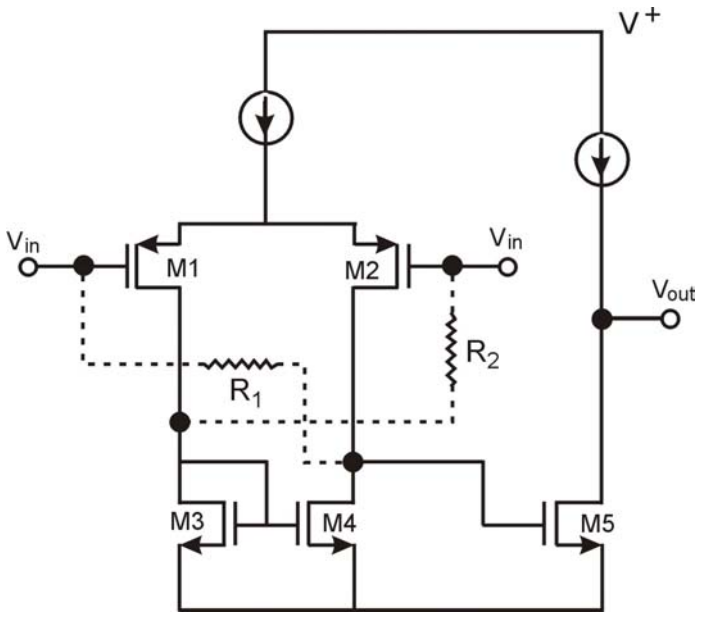

Fig. 3. A simple CMOS operational amplifier.

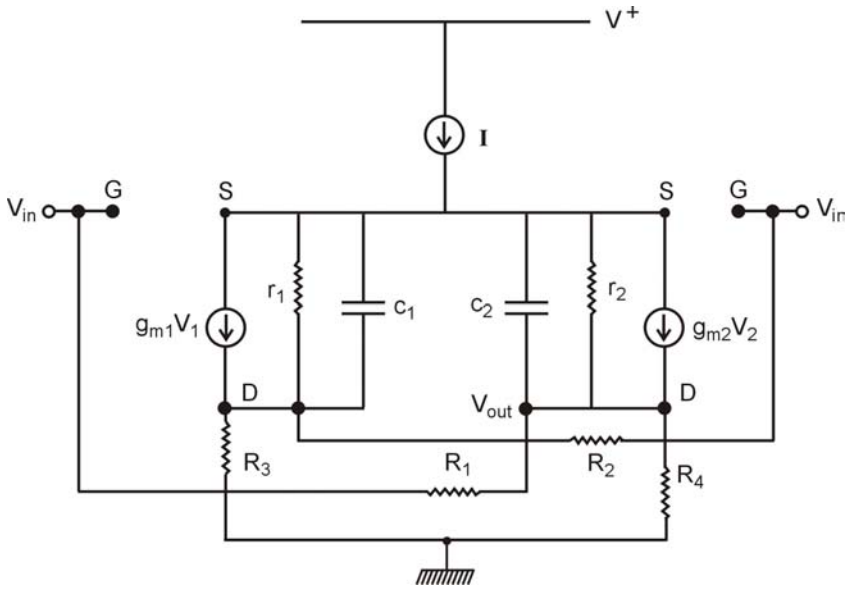

Fig. 4. AC small signal equivalent circuit with positive feedback of Figure 3.

From Figure 4 the gain of the amplifier is, $A_v = \dfrac{\mu R_4}{R_4 + r_i' + r_2'}$

Where r_1' and r_2' are the parallel combination of r_1, c_1 and r_2, c_2; R_3, R_4 are the effective drain resistances of MOSFETs M_3 and M_4 respectively. g_{m1} and g_{m2} are the trans conductances of M_1 and M_2, r_1 and r_2 are the drain resistances of M_1 and M_2, c_1 and c_2 are the drain-source capacitances of M_1 and M_2 respectively. μ is the amplification factor.

$$\therefore r_1' = \frac{r_1}{1 + j\omega c_1 r_1} \text{ and } r_2' = \frac{r_2}{1 + j\omega c_2 r_2}$$

$$\text{Now, } A_v = \frac{\mu R_4}{R_4 + \dfrac{r_1}{1 + j\omega c_1 r_1} + \dfrac{r_2}{1 + j\omega c_2 r_2}}$$

After calculation, the phase factor is

$$\tan\phi = \frac{\omega r_1^2 c_1 \left(1 + \omega^2 c_2^2 r_2^2\right) + \omega r_2^2 c_2 \left(1 + \omega^2 c_1^2 r_1^2\right)}{R_4 \left(1 + \omega^2 c_1^2 r_1^2\right)\left(1 + \omega^2 c_2^2 r_2^2\right) + r_1 \left(1 + \omega^2 c_2^2 r_2^2\right) + r_2 \left(1 + \omega^2 c_1^2 r_1^2\right)}$$

2.2 Calculation of phase factor with positive feedback

In presence of positive feedback resistances, the overall gain of the amplifier will be $A_f = \dfrac{A}{1 + \beta A}$, where β is the feedback ratio and 'A' is gain of the amplifier without positive feedback.

From Figure 4 we can write,

$\beta = \frac{R_i}{R_1 + R_i}$, where R_i is the impedance of the next stage and $R_i \rangle 0$.

Similarly, using positive feedback the phase factor is given by,

$$\tan\phi' = \frac{(R_1 + R_i)\left(1+\omega^2 c_2^2 r_2^2\right)\omega c_1 r_1^2 + (R_1 + R_i)\left(1+\omega^2 c_1^2 r_1^2\right)\omega c_2^2 r_2^2}{\left[\mu R_4\left(1+\omega^2 c_1^2 r_2^2\right)\left(1+\omega^2 c_2^2 r_2^2\right) + R_4\left(1+\omega^2 c_1^2 r_1^2\right)\left(1+\omega^2 c_2^2 r_2^2\right)\right.}$$

$$\left. + r_1\left(1+\omega^2 c_2^2 r_2^2\right) + r_2\left(1+\omega^2 c_1^2 r_1^2\right)\right] R_i +$$

$$\left[R_4\left(1+\omega^2 c_1^2 r_1^2\right)\left(1+\omega^2 c_2^2 r_2^2\right) + r_1\left(1+\omega^2 c_2^2 r_2^2\right)\right.$$

$$\left. + r_2\left(1+\omega^2 c_1^2 r_1^2\right)\right] R_1$$

If $R_1 = \infty$ i.e. without positive feedback,

$$\tan\phi' = \frac{\left(1+\omega^2 c_2^2 r_2^2\right)\left(\omega c_1 r_1^2\right) + \left(1+\omega^2 c_1^2 r_1^2\right)\left(\omega c_2 r_2^2\right)}{R_4\left(1+\omega^2 c_1^2 r_1^2\right)\left(1+\omega^2 c_2^2 r_2^2\right) + r_1\left(1+\omega^2 c_2^2 r_2^2\right) + r_2\left(1+\omega^2 c_1^2 r_1^2\right)}$$

$$= \tan\phi$$

It is evident that $\tan\phi' \langle \tan\phi$, i.e. the phase factor without positive feedback is grater than that with positive feedback. Hence with positive feedback, the delay time reduces compared to that without positive feedback and the speed of operation increases.

The same treatment can be applied to the fully differential amplifier circuit of Figure1 with positive feedback and we will get the similar result. That is with the application of positive feedback, delay produced by each inverter of Figure 2 will decrease and hence the speed of the inverter will increase.

3. Simulated Results

The simulated results of percentage speed improvement with positive feedback resistance for a particular bias current of 25μA is shown in Figure 5. This has been tested by connecting 4 number of such amplifier stages in series and the outputs of the last stage are cross coupled with the inputs of the first stage Figure 2. The frequency of oscillation depends on the number of the inverter stages, the load capacitances and the current level. This graph indicates that the percentage of frequency improvement is maximum for feedback resistance of 33kΩ. For this case an improvement of speed of around 167 % is obtained. Since each amplifier provides push-pull output, the quardrature and multiphase

signals can be obtained from such ring oscillator. Simulated quadrature output waveforms (for feedback resistance of 33kΩ) are shown in the Figure 6. These multiphase signals are very much useful in communication systems.

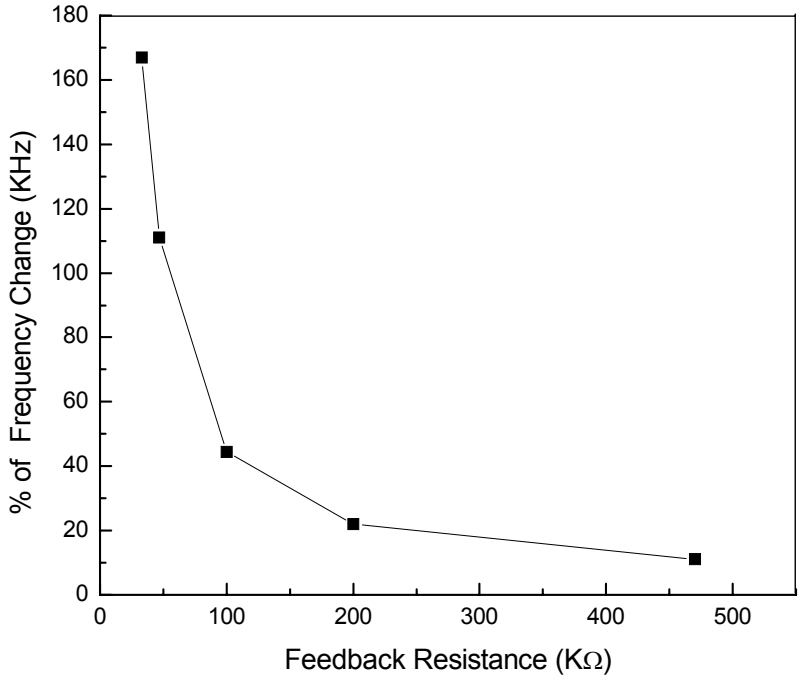

Fig. 5. Percentage of speed improvement with positive feedback resistance.

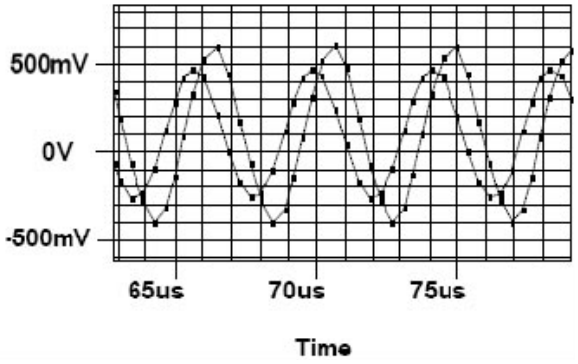

Fig. 6. Simulated quadrature output waveforms of the 4 stage ring oscillator.

Figure 7 shows the percentage of speed improvement with negative feedback resistance. For the same speed improvement, the required feedback resistance is nearly 200kΩ, which is less favourable for integrated circuit fabrication, compare to the fabrication of 33kΩ (used in positive feedback circuit).

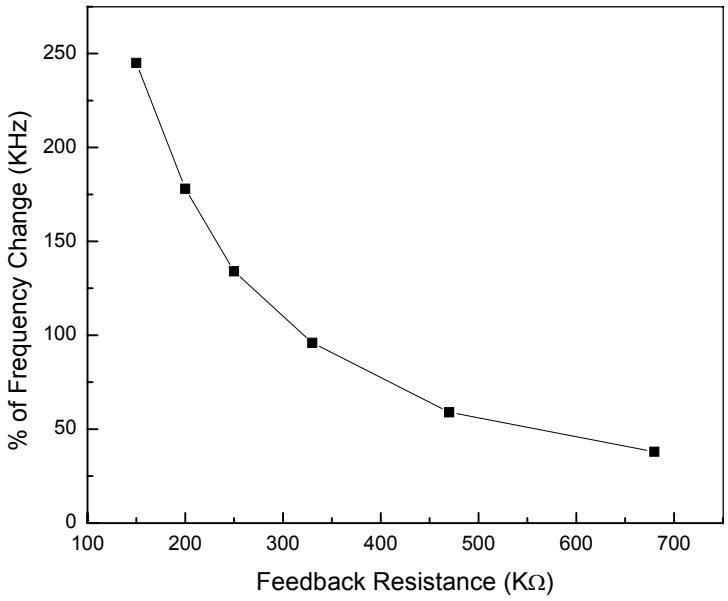

Fig. 7. Percentage of speed improvement with negative feedback resistance.

The variation of frequency of oscillation of the above 4-stage ring oscillator Figure 2 with bias current for a particular feedback resistance of 47 kΩ is shown in the Figure 8. Since the variation is linear over a wide range of current from 25μA to 50μA, the circuit can be very effectively used as a current controlled oscillator (CCO) and is suitable for Phase locked Loop (PLL) applications.

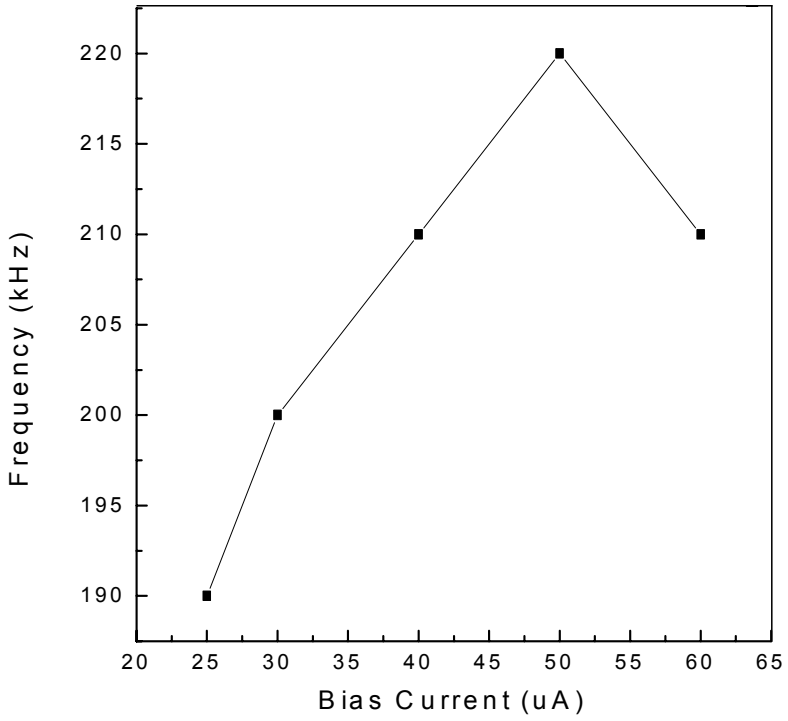

Fig. 8. Frequency change with bias current for a positive feedback resistance of 47 kΩ.

4. Application of the proposed VCO using MOSFETS

In wireless communication systems, e.g. portable voice, data and messaging systems, VCO is an essential part. Frequency synthesizers consisting of VCO, reference oscillator, programmable counters are an integral part of transceivers [4]. Modern communication circuits such as integrated radio paging receivers, QPSK modulators, harmonic generators etc. need quadrature / multiphase outputs. Synchronized / phase locked oscillators are widely used for suppression of noise and interference in an incoming signal [5-9]. Phase locked loops provide multiphase clock signals in digital circuits [10-14]. Multiphase outputs are also required in coherent PSK reception. These multiphase / quadrature outputs may be realized using ring oscillator VCOs as described in Figure 2.

4.1 Multiphase / Quadrature signal generation

The extremely accurate phase tracking capabilities of Charge-pump PLLs help us to generate multiphase non-overlapping clocks [15-19]. For this case, the VCO should

comprise of a multistage tapped delay line that is automatically calibrated to a precise delay per stage [20]. The generation of arbitrary multiphase clocks is possible with proper decoding of the signals from the delay line-taps. In many telecommunication applications (e.g. synchronous detectors) signals that are in quadrature are needed. Such quadrature outputs are generated using the 4 stage ring oscillator VCO as shown in Figure 2. The signals obtained from the outputs of stages X2 and X4 are in phase quadrature and are shown in Figure 6. Note that the frequency of oscillation obtained without positive feedback is only 90 KHz at 25 μA, but with positive feedback (using 33 kΩ resistance) it increases to 240 KHz at the same current.

5. Conclusion

High frequency fully differential CMOS amplifier with positive feedback has been simulated using PSPICE. An even number of such stages has been cross connected to form a ring oscillator. Simulated results showed, due to the application of positive feedback, a maximum of 167 % increase in speed with feedback resistance of 33 kΩ. But in case of negative feedback to gate same speed improvement, the require feedback resistance will be nearly 200 kΩ. Since this feedback resistance is very large, so it is difficult to fabricate in integrated circuits. Hence we have used positive feedback scheme. This improved amplifier can operate with a supply voltage of ± 2.0 Volts. Current tuning characteristics of the ring oscillator is linear over a wide range of current, suitable for PLL applications. The presented circuit is highly suitable for VLSI integration, where the operating speed can be much higher, depending upon device dimension.

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