PG/IVS/ELC-404/12

M.Sc. 4th Semester Examination, 2012

ELECTRONICS

(*VLSI Technology*)

PAPER— ELC-404

(Theory)

Full Marks : 50

Time : 2 hours

Answer **Q. No. 1** and any **three** from the rest

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. (*a*) Name the basic process steps employed in VLSI technology.

   (*b*) Explain the role of O_2 in plasma etching of Si in $CF_4 + O_2$ plasma.

(*c*) Is the choice of crystal orientation critical for Mos devices ? Give answer with reason.

(*d*) Explain the working principle of a negative photoresist.

(*e*) What do you understand by packaging in IC technology ? 2×5

2. (*a*) Name the different methods used to oxidize semiconductors. Explain dry and wet oxidation.

(*b*) Describe with a diagram the various charges associated with thermally oxidized films.

(*c*) How can you grow a thin oxide layer ? $(1 + 3) + 3 + 3$

3. (*a*) What are the advantages of polysilicon in VLSI technology ? How is polysilicon deposited ?

(*b*) How are the silicon nitride films produced ? Mention the importance of silicon nitride in the fabrication of VLSI structure. $(2 + 3) + (3 + 2)$

4. (*a*) Describe latchup effect with diagram.

(*b*) What is a retrograde well ? Write down the advantages of retrograde well over conventional well.

(*c*) Explain gate-engineering technology in the fabrication of CMOS devices. 3 + (2 + 2) + 3

5. (*a*) What do you mean by different levels of packaging ? Name the various attachment methodoligies used for chip-to-package interconnection.

(*b*) Draw the assembly sequence for packages using wire and describe wire bonding technique. (2 + 1) + (2 + 5)

6. (*a*) What do you mean by stick diagrams ? Draw monochrome stick diagrams for NMOS and CMOS inverters.

(*b*) What do you mean by λ-based design rules ? Why it is necessary to follow these rules for the fabrication of VLSI circuits ? State λ-based design rules for diffused and polysilicon layers. (2 + 2) + (2 +2 + 2)

[*Internal Assessment* : 10 Marks]