MCA 1st Semester Examination, 2010

BASIC ELECTRONICS & DIGITAL LOGIC

PAPER – CS/MCA/1103

Full Marks : 100

Time : 3 hours

Answer any **seven** questions

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. What is diode ? Draw the *p-n* junction diode's characteristics curve. Explain the features of Zener diode. Explain centre-tap full wave rectifier. 1 + 4 + 2 + 3

2. (*a*) Minimize the four-variable logic function using K-map.

$$f(A, B, C, D), \sum_m (0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$$

(*b*) Design a Binary to Gray code converter.

(*c*) What is prime implicant. 3 + 5 + 2

3. Compare half adder and full adder. Draw the block diagram of serial adder. Design a *BCD* adder circuit. 2 + 3 + 5

4. (*a*) Convert $Y = (A + B)(A + C)(B + \overline{C})(B + A)$ into canonical POS form.

(*b*) Design a circuit using gates to realise the function

$$Y = (A + BC)(B + \overline{C}A).$$

(*c*) What is parallel adder ? Explain.

(*d*) What is parity generator ? How it is generated ? $2+3+2\frac{1}{2}+2\frac{1}{2}$

5. What is PLA ? Using four variable map

$$Q = m_0 + m_2 + F\,m_6 + m_7 + E\,m_8 + E\,m_{10} + m_{12} + m_{14} + F\,m_{15}$$

Convert T Flip-Flop to JK Flip-Flop. Explain JK M/S Flip-Flop with timing diagram. 1 + 2 + 4 + 3

6. (*a*) How many memory locations are addressed using 18 address bits ?

(*b*) How many address bits are needed to operate a 2K × 8 bit ROM memory ?

(*c*) How does a static RAM cell differ from a dynamic RAM cell ?

(*d*) Draw the basic circuit of a ROM cell and explain its working. 1 + 1 + 2 + 6

7. (*a*) What is doping ?

(*b*) What is extrinsic semiconductor ? How it differs from intrinsic semiconductor.

(*c*) Explain Fermi-Dirac distribution function and point out Fermi level and its position on the Energy Band (EB) diagram for intrinsic, *p*-type and *n*-type semiconductor ? 2 + 3 + 5

8. Design a circuit diagram for ADC. Design a AND gate and OR gate using DRL. Design a NOT gate using RTL. 5 + 3 + 2

9. Design a full subtractor using Multiplexer. Draw the circuit diagram of ODD-PARITY generator. Implement the following function with a multiplexer: 4 + 3 + 3

$$F(A, B, C, D) = \Sigma (0, 1, 3, 4, 8, 9, 10).$$

10. Design a ROM which has the address and corresponding data given below:

Address	Data
00	10111
01	11100
10	10000
11	10100

Design a RAM. Compare the PROM, EPROM and E^2PROM. 4 + 4 + 2

[*Internal Assessment* : 30 Marks]