2012

M.Sc.

1st Semester Examination

PARALLEL ARCHITECTURE

PAPER—COS-102

Full Marks : 50

Time : 2 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

All notations have their usual meaning.

Module—1

(Marks : 25)

Answer any *two* questions.

1. Consider a pipeline that has 5 stages, (i) Instruction fetch – 200 ps, (ii) Instruction decode – 100 ps, (iii) Instuction execution – 200 ps, (iv) memory read – 200 ps, and (v) register write – 100 ps.

(i) If the machine is not pipelined, but the latencies for the various operations involved in instruction fetch and execute are the same as above, what is the latency of a single instruction?

(ii) What is the latency of an instruction flowing through the pipeline?

(iii) What is the idealized speedup? (Ignore pipeline fill and pipeline drain) 4+4+2

2. Consider the sequences of MIPs instrutions :

```
lw  $1, 40($2)
add $2, $3, $4
add $1, $1, $2
sw  $1, 20($2)
```

(i) Identify all the data dependencies in the above instruction, whether or not they cause any hazards or stalls.

(ii) Suppose we execute these instructions on a processor with a 5-stage pipeline with forwarding. Are there any hazards in the above sequence of instrutions that will require the pipeline to stall because they can't be handled by the forwarding mechanisms? If so, where are they and why is the stall needed? 6+4

3. (a) Differentiate between :

(i) Arrary Processor and Multi Processor.

(ii) RISC and CISC.

(iii) What is vector processor? What are the advantages of vector processor?

$(2\frac{1}{2}+2\frac{1}{2})+(2+3)$

[Internal Assessment — 5 marks]

Module—2

(*Microprocessor*)

(Marks : 25)

Answer any *two* questions : 2×10

4. (a) How many functional units does 8086 contain? Discuss them in brief.

(b) What are LOCK and $\overline{\text{LOCK}}$?

(c) Why instruction queue is introduced in 8086?

(d) Write the functions of control flags (F). 4+2+2+2

5. (a) Discuss the important features of 80286.

(b) Describe the hardware interrupts of 8086.

(c) Draw the timing diagram of Intel 8086 for memory read in minimum mode.

(d) Describe Based Indexed Addressing mode. 2+2+4+2

6. (a) What are different operating mode of 8255?

(b) Explain how the 8237 DMA controller transfer 64K bytes of data per channel with eight address lines.

(c) What is the effect of execution the instruction?

ADD AX, [BX + 08] 4+4+2

[Internal Assessment — 05]

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