2015

MCA

1st Semester Examination

BASIC ELECTRONICS & DIGITAL LOGIC LAB

(PRACTICAL)

PAPER—MCA-107

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary,

Answer any *one* question (*Lottery Basis*). 1×50

1. Design NOT, OR, AND, XOR, XNOR gates using minimum number of NAND gates.
2. Design NOT, OR, AND, XOR, XNOR gates using minimum number of NOR gates.
3. Construct a circuit to convert Binary number to corresponding Gray code & odd parity generator.
4. Design a circuit to convert BCD to Excess 3.

5. Design a four bit adder & 2's complement subtractor using IC 7483 and XOR gates.

6. Design Full adder and Full subtractor using 8:1 MUX.

7. Design BCD address using 7483 IC.

8. Design Full adder & Full subtractor using 4:1 MUX.

9. Construct clocked SR, D & JK flip-flop using NAND gates. Verify its operation.

10. Design a circuit to convert Gray to Binary & even parity generator.

11. Design 4 bit ripple counter & then MOD 10 counter.

12. Design 4 bit ripple counter & then MOD 12 counter.

Marks Distribution

Theory	:	10
Circuit diagram	:	10
Implementation	:	10
Verification	:	10
Discussion	:	05
LNB	:	05
Viva Voce	:	20
Internal	:	30