2015

MCA

1st Semester Examination

BASIC ELECTRONICS AND DIGITAL LOGIC

PAPER-MCA-103

Full Marks: 100

Time: 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any seven questions.

1.	(a)	Define the term 'doping'.	2
	(b)	Distinguish between a metal, an insulator, a a semiconductor in light of band theory.	no 3
	(c)	Define ripple factor. Calculate its value for half wa and full wave rectifier.	3
	(d)	Describe the terms capacitor input filter and induct	(O
		immit filton	2

(Turn Over)

2.	(a)	Establish the relation $I_C = \beta I_B + (1 + \beta)I_{CBO}$.			
		Symbols have their usual meanings.	2		
. •	(b)	Explain the output characteristics of transistor in CE configuration.	a n-p-n		
	(c)	For a transistor $\alpha = 0.998$ and voltage d 8 K Ω which is connected in the collector 8 volt.	-		
		Find the base current for common emitter of	onnection.		
3.	(a) Explain briefly the operation of a Bridge rectifier with diagram. What are the advantages and disadvantages of bridge rectifier over full wave center taped rectifier using diodes? 3+2				
	(b)	Derive the expression for the OPAMP integrator and draw the circuit diagram.	used as a		
4.	(a)	What is Q point? Why does the Q point temperature?	vary with 2+2		
	(b)	What is dc load line?	1		
	(c)	Write short note on hybrid parameters of a	transistor. 5		
5.	(a)	What is Gray Code? Why it is important	.? 2		
	(b)	Design a Gray to Binary Code converter.	5		
C/15/MCA/1 st Seme./MCA-103 (Continued)					

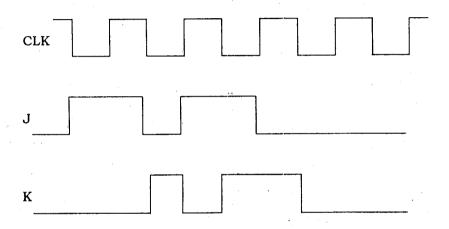
 $\overline{\overline{AB} + ABC} + A(B + AB)$

- **6.** (a) Express the function $Y = A + \overline{B}C$ in
 - (a) canonical SOP and (b) canonical POS form. 5
 - (b) Convert the Gray code 10110101 into binary code, BCD code and excess 3 code.
 - (c) Represent the following numbers in two's complement from -7 and +7.
- 7. (a) With the help of a logic diagram, explain a parallel adder / subtractor using 2's complement system. 5
 - (b) Implement the function $F(a,b,c) = ab + \overline{b}c$ using a 4:1 MUX.
- 8. (a) Design full subtractor using 3×8 decoder. 4
 - (b) Show how the J-K flip-flop can be operated as a toggle flip-flop.
 - (c) What is race-around condition? What is the basic difference between shift register and counter?

 $\left(1\frac{1}{2}+1\frac{1}{2}\right)$

9. (a) The waveforms shown in figure below are applied to (a) a Positive edge triggered JK flip-flop, (b) a Negative edge triggered JK flipflop.

Draw the output waveform in each case: 3+3



- (b) Design and explain 2-bit magnitude comparator. 4
- 10. (a) Design with proper circuit diagram asynchronousMOD 10 counter using J-K flip-flop.5
 - (b) Design a type D counter that goes through states 0,1,3,4,0, ... The undesired (unused) states must be always goes to (000) on the next clock pulse. 5

Internal Assessment: 30