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A New Method of Realization of Four-Quadrant Analog Multiplier using Operational Amplifiers and MOSFETs

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ABSTRACT

In this article, we present a new method of realization of a four-quadrant analog multiplier using operational amplifiers (OP-AMPs) and MOSFETs. The realisation is based on the quadric nature of current of MOSFET operating in triode region. The multiplier can be derived from the proposed configuration with using either bipolar or complementary metal-oxide-semiconductor (CMOS) OP-AMPs. It can be used effectively with a wide range of supply voltages down to ± 1 V and can multiply over the full scale of the supply voltage if the OP-AMPs used are rail-to-rail low voltage OP-AMPs. The performances of the proposed multiplier are tested through PSPICE (Cadence 16.6) simulation using TSMC 0.35 µm CMOS process parameters and are found to be in close agreement with the theoretical predictions. Simulation results of the derived multiplier demonstrate a − 3 dB bandwidth of 9.6 MHz, a THD less than 1.21%, and an output referred noise less than 14 nV/√Hz at 1 kΩ load condition. The maximum power consumption of the circuit is 0.75 mW. The applications of the proposed multiplier as a squarer, an amplitude modulator and a frequency doubler are also included.

Keywords: Four-Quadrant Analog Multiplier, Operational Amplifier (OP-AMP), Amplitude Modulator (AM), Squarer Circuit, Frequency Doubler.

1. Introduction

Four-Quadrant analog multiplier is a key element in the field of analog signal processing, telecommunications and electronic systems. Modulation, demodulation, rectification, frequency translation, automatic gain control (AGC), squaring and square rooting of signals etc., are usually performed using this circuit [1-2]. There are different approaches to implement analog multiplier, such as, using modified Gilbert cell [3], based on trans-linear property of bipolar junction transistors or MOSFETs operating in saturation region [4-7], using switched-capacitor [8] and based on current-voltage characteristics of MOSFETs in triode-region [9]. But, these approaches are realised for the specific purpose and are not available in commercial integrated circuit (IC) form. Many circuit designers use different high-performance active building blocks (ABBs), namely, second generation current conveyor (CCII) [1], current controlled current conveyors (CCCII)

[10], operational trans-conductance amplifiers (OTA) [11], operational trans-resistance amplifiers (OTRA) [12], differential difference current conveyors (DDCC) [13], current differencing buffered amplifiers (CDBA) [14, 15], current controlled current differencing buffer amplifiers (CCCDBA) [16], current controllable current conveyor trans-conductance amplifiers (CCCCTA) [17], current differencing trans-conductance amplifiers (CDTA) [18], current controlled current differencing trans-conductance amplifiers (CCCDTA) [2], etc., to make their multiplier circuits. But those circuits are costly. In the design of an electronic circuit, we also think of its economical aspect, along with its flexibility of design.

On the other hand, an operational amplifier (OP-AMP) is a commercially available, low-cost and high performance device and it is usually used as a basic circuit building block in analog circuits and system applications. The use of OP-AMP in the realisation of the analog multiplier will provide the structure of high performance at low cost and simple configuration. From literature survey, it is found that a no of implementations of OP-AMP based multiplier circuits have been reported [19-24]. However, careful observed study shows that those circuits are not free from limitations. The circuit reported in [19] uses as much as five OP-AMPs and eleven resistors. Using three OP-AMPs, Petchmaneelumka et al., presented an analog multiplier circuit in [20] but the circuit needed eighteen resistors. The circuit informed by Riewruja and Rerkratn [21] uses three OP-AMPs and sixteen resistors. The multiplier/divider circuits reported in [22] and [23] employ a single OP-AMP and eight MOSFETs but both positive and negative feedback are used in the circuits, thereby hampering the stability of the circuits. In [24] Ismail et al., introduced a multiplier/divider circuit using two OP-AMPs and six MOSFETs but the circuit used a sufficiently large supply voltage of ± 6 V.

In this paper, a new method of realization of a four-quadrant analog multiplier using operational amplifiers (OP-AMPs) is described. The proposed circuit employs three OP-AMPs, two MOSFETs and six resistors only. The realisation is based on the quadric nature of current of MOSFET operating in linear region. Both the bipolar and CMOS OP-AMPs can be used to realise the four-quadrant analog multiplication using the proposed structure. The proposed circuit provides low cost, simple configuration and good performance. The other important advantages of this circuit are as follows - it can be used with a wide range of supply voltages even from ± 1 V and it can multiply over the full scale of the supply voltage if the OP-AMPs used are rail-to-rail low voltage OP-AMPs. The workability of the derived multiplier is verified by PSPICE (Cadence 16.6) simulation using 0.35 μm TSMC CMOS process parameters. It is found that the simulated results are in close agreement with the mathematically predicted results. The performances of the circuit as amplitude modulator, squarer and frequency doubler are also tested.

2. Circuit description

The proposed four-quadrant analog multiplier circuit is shown in Figure 1**.** The OP-AMPs A_1 and A_2 are assumed to be well matched such that the quiescent current and the bias current of the OP-AMPs are equal. The MOSFETs M_1 and M_2 are also assumed to be matched and biased to operate in triode region. Thus the expression for drain current for the MOSFETs is given by [12]:

$$I_d = K\frac{W}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \quad (1)$$

where K is trans-conductance; W and L are the channel width and length of the MOSFET respectively. The other terms are of their usual meaning.

Since the source terminals of the MOSFETs M_1 and M_2 are virtually ground, thus using equation (1), the current I_1 and I_2 can be expressed as:

$$I_1 = K\frac{W}{L}\left[(V_G + v_2 - V_t)v_1 - \frac{v_1^2}{2}\right] \quad (2)$$

$$I_2 = K\frac{W}{L}\left[(V_G - V_t)v_1 - \frac{v_1^2}{2}\right] \quad (3)$$

If we assume $R_1 = R_2 = R$, then the output voltage of the OP-AMPs A_1 and A_2 i.e. v_{O1} and v_{O2} can be expressed as:

$$v_{O1} = -RK\frac{W}{L}\left[(V_G + v_2 - V_t)v_1 - \frac{v_1^2}{2}\right] \quad (4)$$

$$v_{O2} = -RK\frac{W}{L}\left[(V_G - V_t)v_1 - \frac{v_1^2}{2}\right] \quad (5)$$

The OP-AMP A_3 along with resistors R_3–R_6 form a differential amplifier, where $R_3 = R_5 = R_i$, and $R_4 = R_6 = R_f$. The routine circuit analysis shows that the output voltage of the proposed circuit can be expressed as:

$$v_O = K\frac{W}{L}\left(\frac{RR_f}{R_i}\right)(v_1 v_2) = K_m(v_1 v_2) \quad (6)$$

where $K_m = K\frac{W}{L}\left(\frac{RR_f}{R_i}\right)$, is the multiplication gain. From equation (6), it is seen that the proposed topology can be used as a four-quadrant analog multiplier.

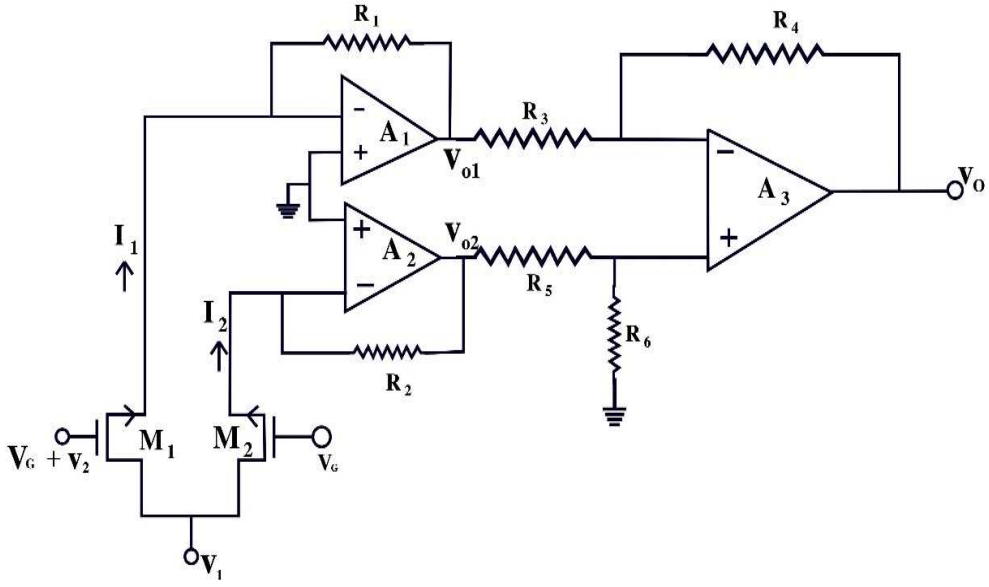


Figure 1. The proposed four-quadrant analog multiplier circuit.

3. Simulation results

Although the proposed circuit can be derived from either bipolar or CMOS OP-AMPs and it can be used effectively with a wide range of supply voltages down to ± 1 V, but for the space convenience, in this article, we demonstrate only the simulation results of the proposed circuit, constructed by using the OP-AMPs, as in [25] with supply voltage ± 1 V. The resistors used in the circuit are chosen as $R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = 1$ kΩ with 1% tolerance and the transistors M_1–M_2 are used with aspect ratios having $W/L = 2.8\mu/0.35\mu$. Control voltage V_G is taken as 1 V. TSMC 0.35 μm CMOS model parameters are used for the simulation purpose. Figure 2 depicts the dc transfer characteristics of the proposed circuit as multiplier. Here, the input voltage v_2 is swept from −1 V to + 1 V while v_1 is varied from − 400 mV to + 400 mV in steps of 100 mV. It confirms that the proposed circuit acts as a four quadrant multiplier.

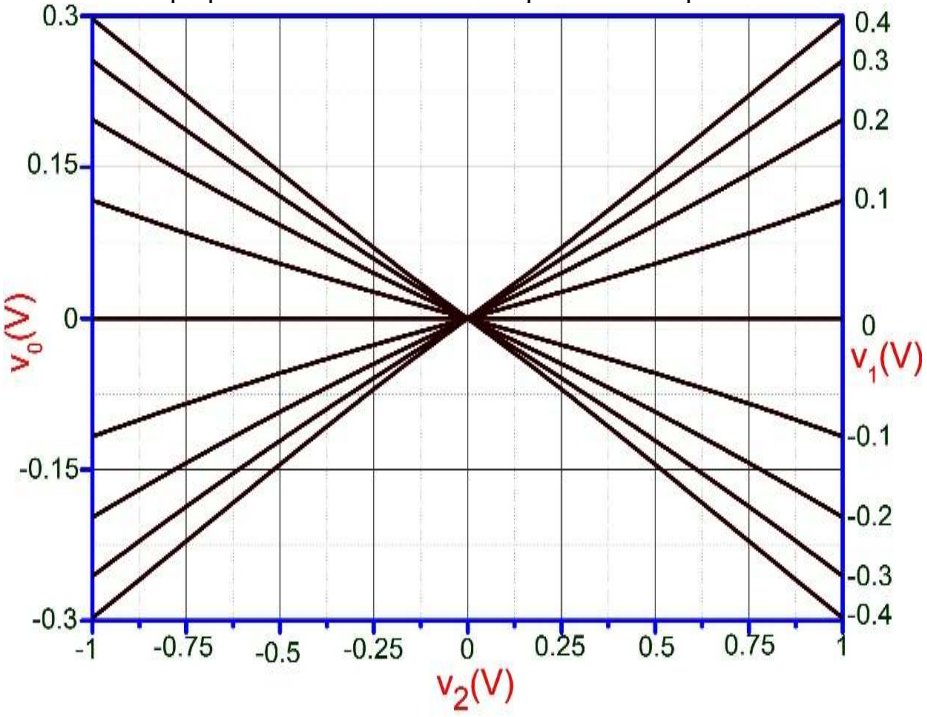


Figure 2. DC transfer characteristic (v_2 is swept, v_1 changed in steps).

Figure 3 shows the frequency response characteristic of the proposed multiplier. In this case, voltage v_2 is kept constant at 200 mV while v_1 is taken as an AC source having amplitude 250 mV. The − 3 dB bandwidth is found to be about 9.6 MHz. Figure 4 shows the output referred noise voltage. It is found to be less than 14 nV/√Hz at 1 kΩ load condition.

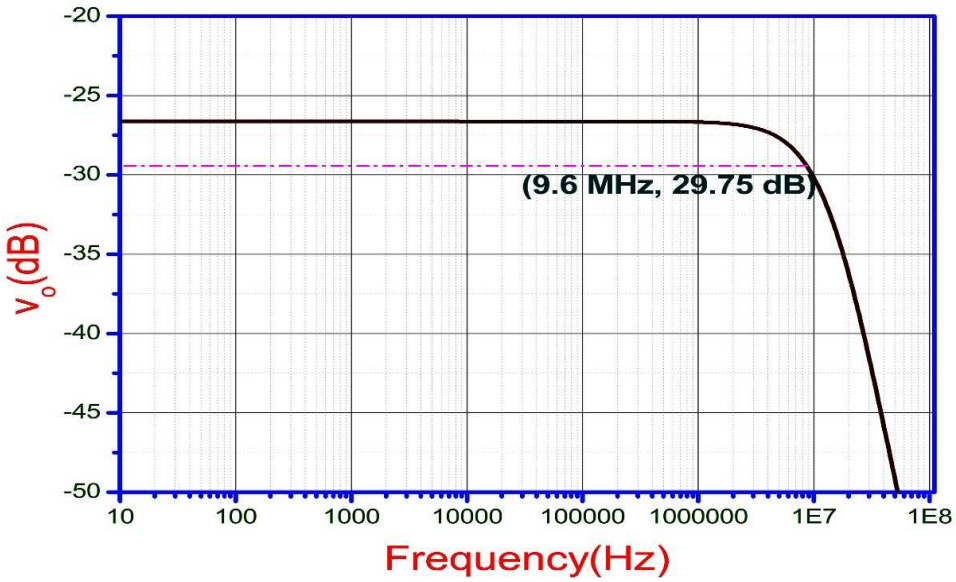


Figure 3. AC characteristic of the proposed multiplier.

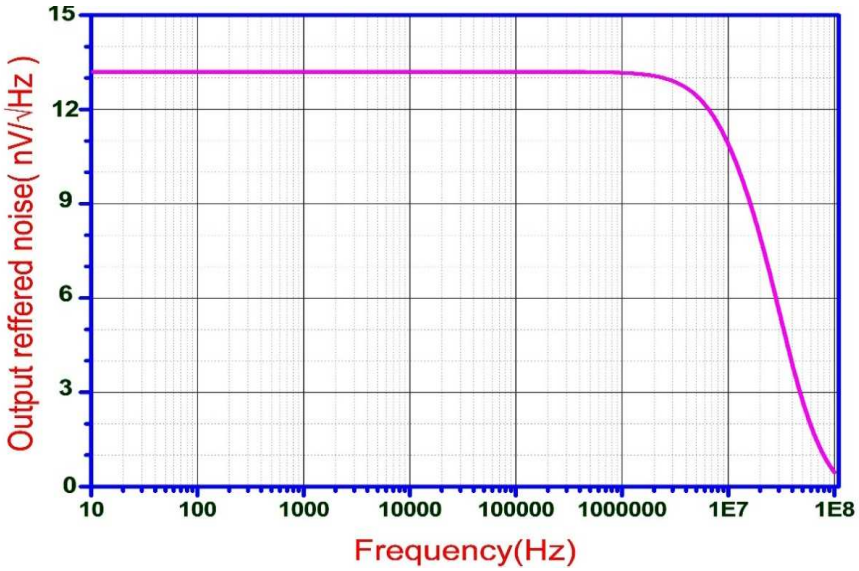


Figure 4. The output referred noise spectral density of the multiplier output at 1KΩ load condition.

Figure 5 shows the variation of total harmonic distortion (THD) with respect to the variation of amplitude of the input signal with frequency (1 kHz, 10 kHz and 50 kHz) as a parameter. For this purpose a sinusoidal signal of varying amplitude with frequency 1 kHz/ 10 kHz / 50 kHz is taken as v_1 where a constant 200 mV DC voltage is applied to v_2. It shows that the maximum THD does not exceed 1.21% for the entire input range.

Total power consumption of the proposed multiplier circuit is 0.75 mW when $v_1 = v_2 = 0$ V.

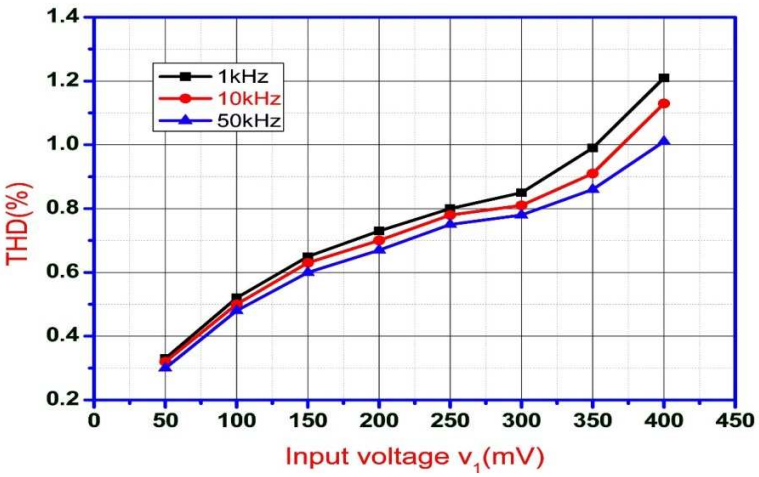
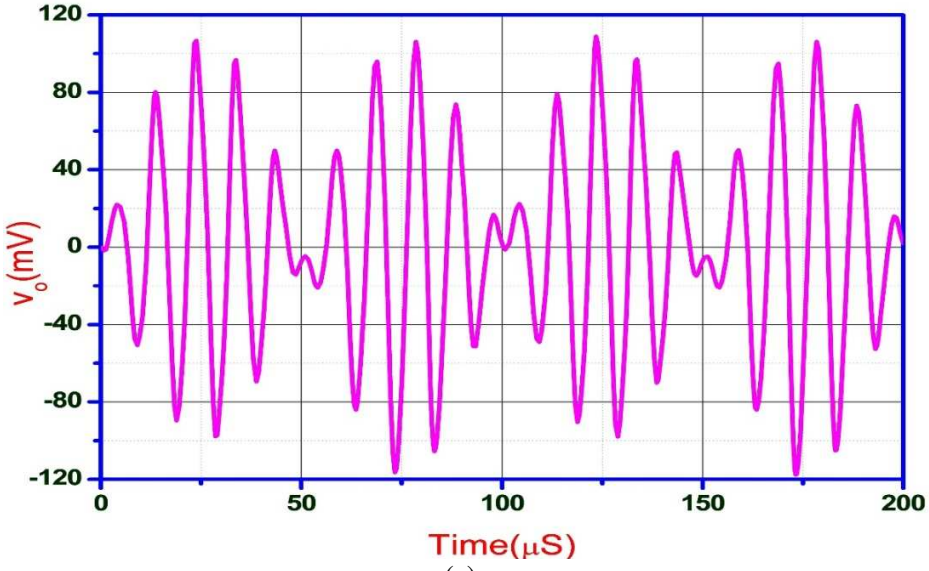


Figure 5. Variation of THD with the amplitude of the input signal (v_1).

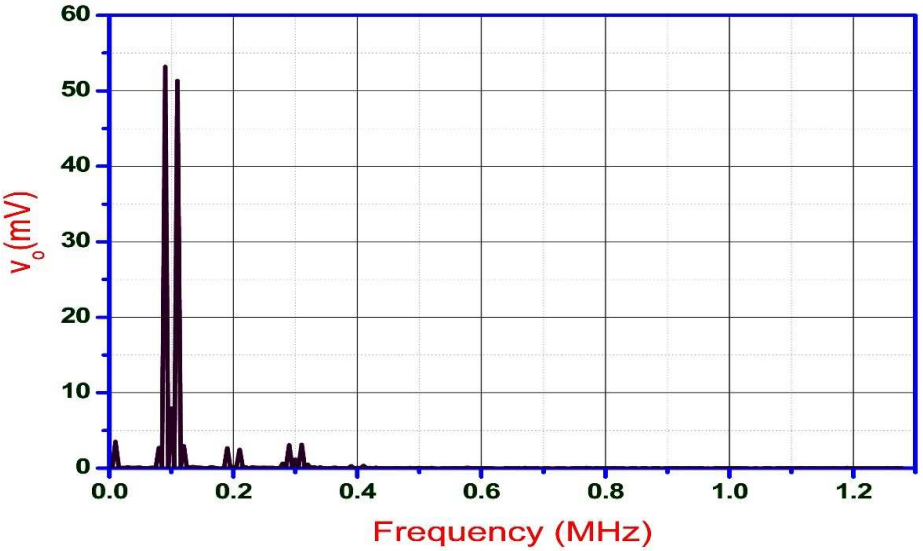
4. Application example

4.1. Amplitude modulator

The proposed multiplier circuit, being four-quadrant multiplier, can be used as an amplitude modulator (AM). To verify the operation of the proposed configuration as a modulator, a 10 kHz signal with 300 mV amplitude is multiplied by 500 mV, 100 kHz signal. Figure 6 confirms about the modulation function. Figure 6(a) shows the time domain response of the modulator. The frequency spectrum is shown in Figure 6(b).



(a)

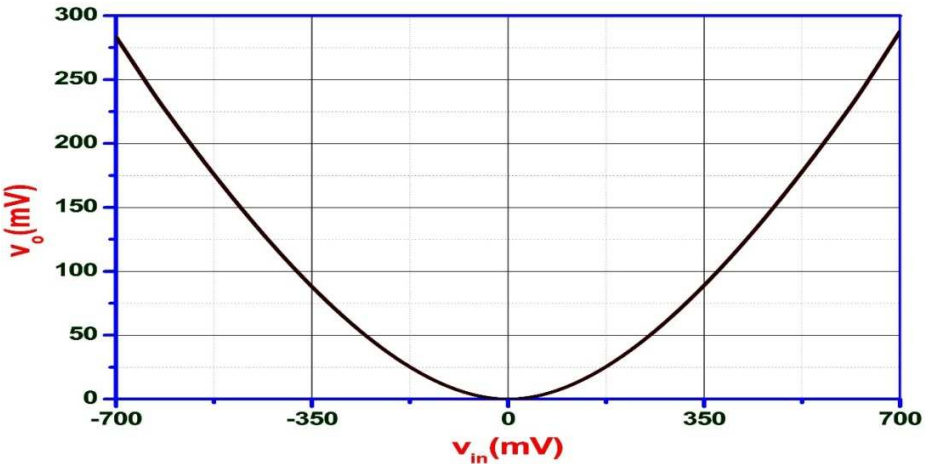


(b)

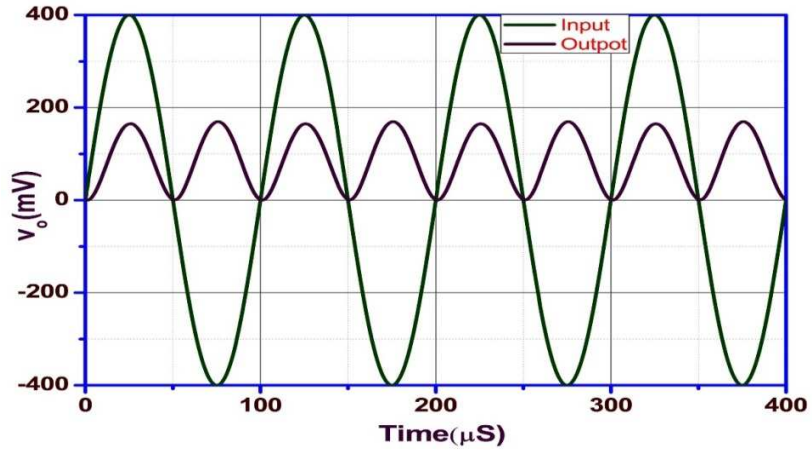
Figure 6. Simulation result of the reported configurations as an amplitude modulator (a) time domain response (b) frequency spectrum.

4.2. Squarer

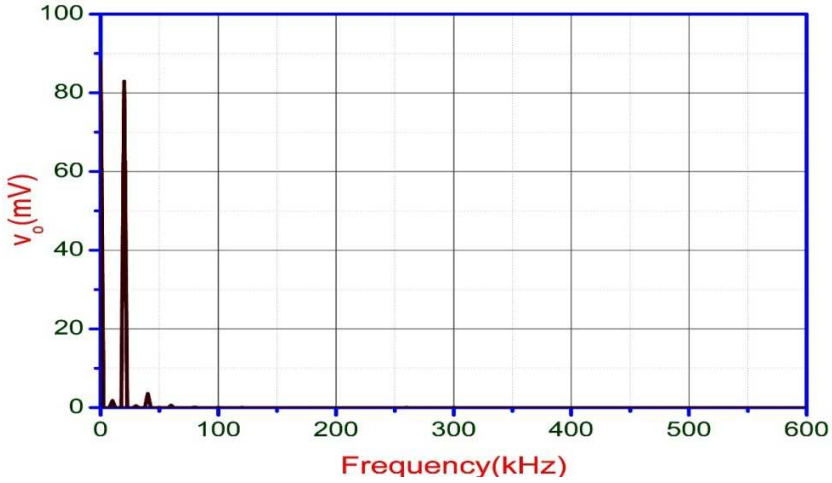
The proposed circuit can also be used as a squarer circuit if we take $v_1 = v_2 = v_{in}$. Figure 7(a) displays the square transfer characteristics of the reported configuration where v_{in} is varied from −700 mV to + 700 mV. The observed input and output of the squarer is shown in Figure 7(b) and the spectrum of the squared output is shown in Figure 7(c) when the input signal is taken as a 400 mV, 10 kHz sinusoid.



(a)



(b)

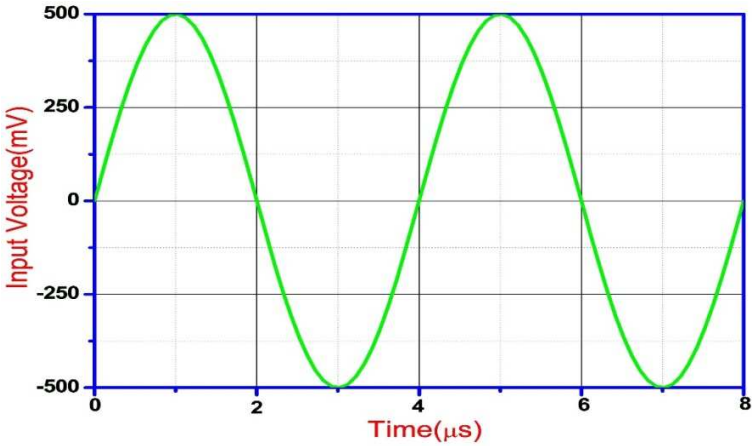


(c)

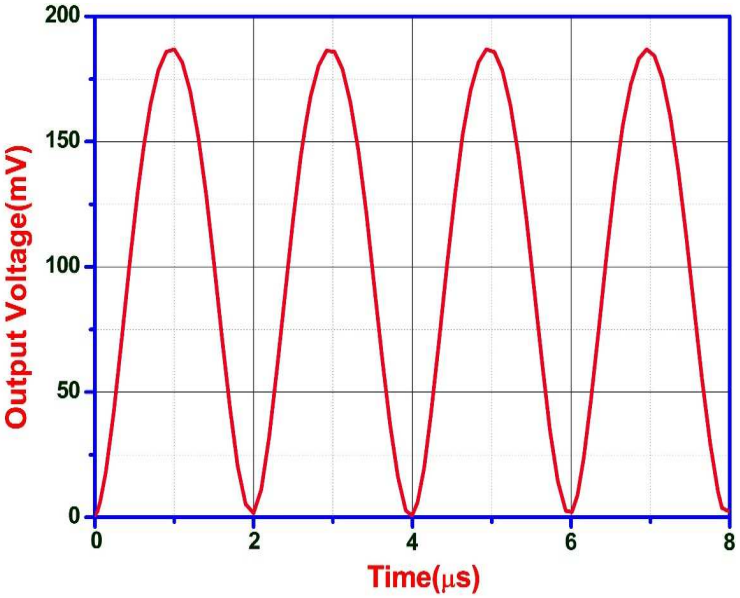
Figure 7. Simulation results of the proposed cell as a squarer
(a) transfer characteristics (b) time response (c) frequency spectrum.

4.3. Frequency doubler

Being a four-quadrant multiplier, the proposed circuit can be used as a frequency doubler. Figure 8 shows that when a 500 mV, 250 kHz sinusoidal signal is used as input signal we get a 187 mV, 500 kHz signal at the output. Thus we may conclude that the proposed circuit can be efficiently used as a frequency doubler.



(a)



(b)

Figure 8. Simulation result of the reported configurations as a frequency doubler (a) input (b) output.

5. Conclusion

An OP-AMP based four-quadrant analog multiplier circuit has been proposed. Both the bipolar and CMOS OP-AMPs can be used to realise the four-quadrant analog multiplication using the proposed structure. It provides low cost, simple configuration and good performance. It has been investigated that the proposed circuit can operate with a wide range of supply voltages down to ± 1 V and can multiply over the full scale of the supply voltage if the OP-AMPs used are rail-to-rail low voltage OP-AMPs. The performances of the derived multiplier are verified by PSPICE simulation results.

Simulation results show a THD less than 1.21%, a − 3 dB bandwidth of 9.6 MHz, an output referred noise less than 14 nV/√Hz, and a maximum power dissipation of 0.75 mW for the proposed circuit. The workability of the proposed circuits as amplitude modulator, squarer and frequency doubler are also described.

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